Mockingbird_CML Schematic

2019/12/09

REV : SC

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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Title	Cover Page	
Size A4	Document Number: Mockingbird CML	Rev SC
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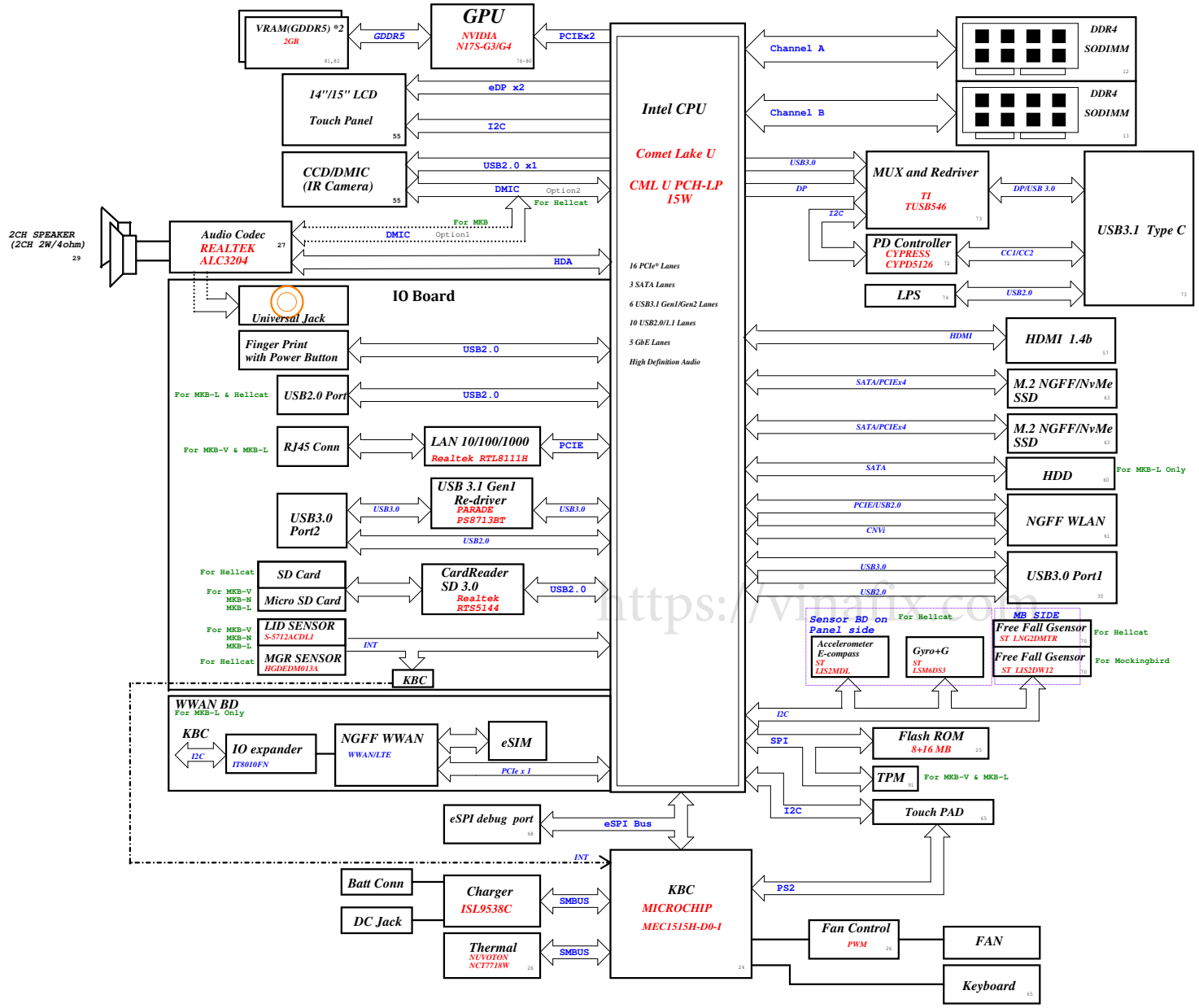
Mockingbird N/V/L/HellCat CML Block Diagram



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Title
Block Diagram
Size: Custom
Document Number: Mockingbird CML
Rev: SC
Date: Monday, December 09, 2019
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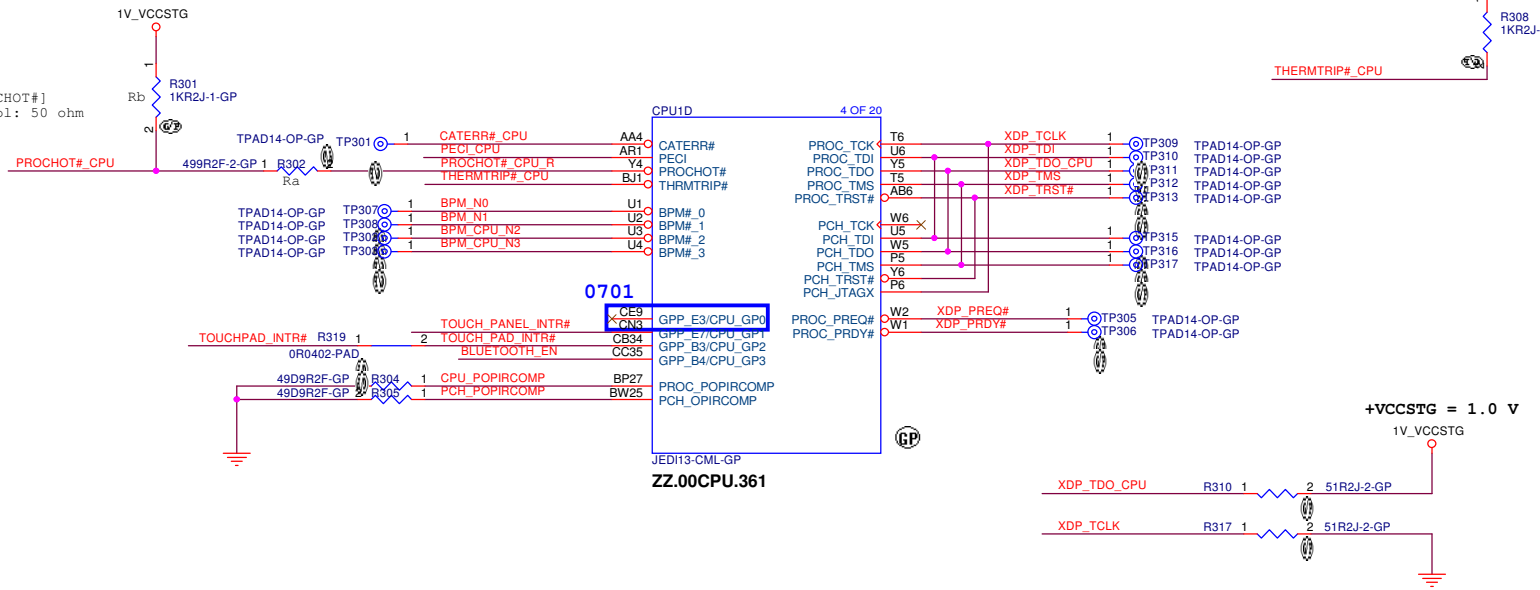
SSID = CPU

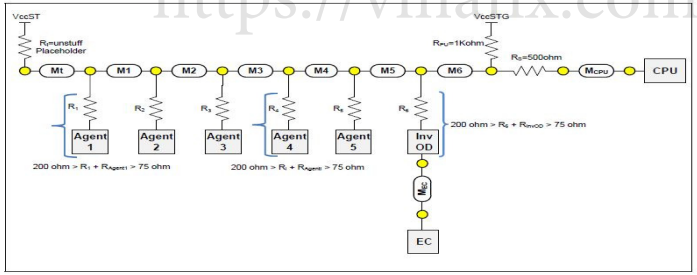
[24] PECI_CPU
[24,44,46] PROCHOT#_CPU
[55] TOUCH_PANEL_INTR#
[24,65] TOUCHPAD_INTR#
[61] BLUETOOTH_EN

[PECI] and [PROCHOT#]
Impedance control: 50 ohm



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

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Title: CPU (THML/JTAG)
Size: A3
Document Number: Mockingbird CML
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SSID = CPU

DP to HDMI2.0

[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N2
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N3
[57] HDMI_DDI_TX_P3

[57] HDMI_HPD_CPU

[57] HDMI_SCL_CPU
[57] HDMI_SDA_CPU

DP for Type-C Mux

[73] DP2_DDI_TX_N0
[73] DP2_DDI_TX_P0
[73] DP2_DDI_TX_N1
[73] DP2_DDI_TX_P1
[73] DP2_DDI_TX_N2
[73] DP2_DDI_TX_P2
[73] DP2_DDI_TX_N3
[73] DP2_DDI_TX_P3

[73] DP2_AUX_CPU_P
[73] DP2_AUX_CPU_N

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1

[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P

[55] eDP_HPD_CPU

[72,73] DP1_HPD_CPU

[24] L_BKLT_EN
[55] L_BKLT_CTRL
[55] EDP_VDD_EN

[15] GPP_H17_STRAP

[55] IR_CAM_DET#

1.65GT Length 6.5" (3VIA)

DP to HDMI1.4b

3D3V_S0
RN401
HDMI_SCL_CPU
HDMI_SDA_CPU
SRN2K2J-1-GP

DP for Type-C Mux

3D3V_S0
SRN2K2J-1-GP
CPU_DP2_CTRL_DATA
CPU_DP2_CTRL_CLK
RN403
10KR2J-3-GP
R407
IR_CAM_DET#
R408
CAM_SHUTTER#
Hellcat
10KR1F-GP

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

CPU1A
1 OF 20

HDMI_DDI_TX_N2 AL5
HDMI_DDI_TX_P2 AL6
HDMI_DDI_TX_N1 AJ5
HDMI_DDI_TX_P1 AJ6
HDMI_DDI_TX_N0 AF6
HDMI_DDI_TX_P0 AF5
HDMI_DDI_TX_N3 AE5
HDMI_DDI_TX_P3 AE6
DDI1_TXN_0
DDI1_TXP_0
DDI1_TXN_1
DDI1_TXP_1
DDI1_TXN_2
DDI1_TXP_2
DDI1_TXN_3
DDI1_TXP_3

DP2_DDI_TX_N0 AC4
DP2_DDI_TX_P0 AC3
DP2_DDI_TX_N1 AC1
DP2_DDI_TX_P1 AC2
DP2_DDI_TX_N2 AE4
DP2_DDI_TX_P2 AE3
DP2_DDI_TX_N3 AE1
DP2_DDI_TX_P3 AE2
DDI2_TXN_0
DDI2_TXP_0
DDI2_TXN_1
DDI2_TXP_1
DDI2_TXN_2
DDI2_TXP_2
DDI2_TXN_3
DDI2_TXP_3

EDP_TXN_0 AG4
EDP_TXP_0 AG3
EDP_TXN_1 AG2
EDP_TXP_1 AG1
EDP_TXN_2 AJ4
EDP_TXP_2 AJ3
EDP_TXN_3 AJ2
EDP_TXP_3 AJ1
eDP_TX_CPU_N0
eDP_TX_CPU_P0
eDP_TX_CPU_N1
eDP_TX_CPU_P1

Length 2"-10" (2VIA)
Cable Length 4"-15"

EDP_AUX_N AH4
EDP_AUX_P AH3
eDP_AUX_CPU_N
eDP_AUX_CPU_P

Length 10" (3VIA)

DISP_UTILS AM7

DDI1_AUX_N AC7
DDI1_AUX_P AC6
DDI2_AUX_N AD4
DDI2_AUX_P AD3
DDI3_AUX_N AG7
DDI3_AUX_P AG6
DP2_AUX_CPU_N
DP2_AUX_CPU_P

TYPE-C MUX

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6
GPP_E17/EDP_HPD/DISP_MISC4 CM7
HDMI_HPD_CPU
DP1_HPD_CPU_R
SIO_EXT_SMI#
IR_CAM_DET#
eDP_HPD_CPU

EDP_BKLTEN CK11
EDP_VDDEN CG11
EDP_BKLTCTL CH11
L_BKLT_EN
EDP_VDD_EN
L_BKLT_CTRL

1V_VCCIO
R401
24D9R2F-L-GP
eDP_RCOMP_CPU AM6
DISP_RCOMP

HDMI_SCL_CPU CC8
HDMI_SDA_CPU CC9
GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA

CPU_DP2_CTRL_CLK CH4
CPU_DP2_CTRL_DATA CH3
GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA

TPAD14-OP-GP TP402
TPAD14-OP-GP TP403
CAM_SHUTTER# CP4
GPP_E23 CN4
IGC6_THM_DIS# CR26
GPP_H17_STRAP CR28
GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA
GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA

JEDI13-CML-GP

ZZ.00CPU.361

3D3V_S0
SIO_EXT_SMI#
R402
10KR1F-GP

Add RTC Gen 9 reset circuit_20170814
leakage issue

3D3V_S5_PCH
R406
10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
R405
10KR2J-3-GP
RTC_RST
Q401
DP1_HPD_CPU_R
DP1_HPD_CPU
CPU_DP_HPD_P
RTC_RST
common part
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

RTC Gen 9 reset circuit_20170814
DP1_HPD_CPU_R
R403
100KR2J-1-GP

DP for Type-C Mux

<Core Design>

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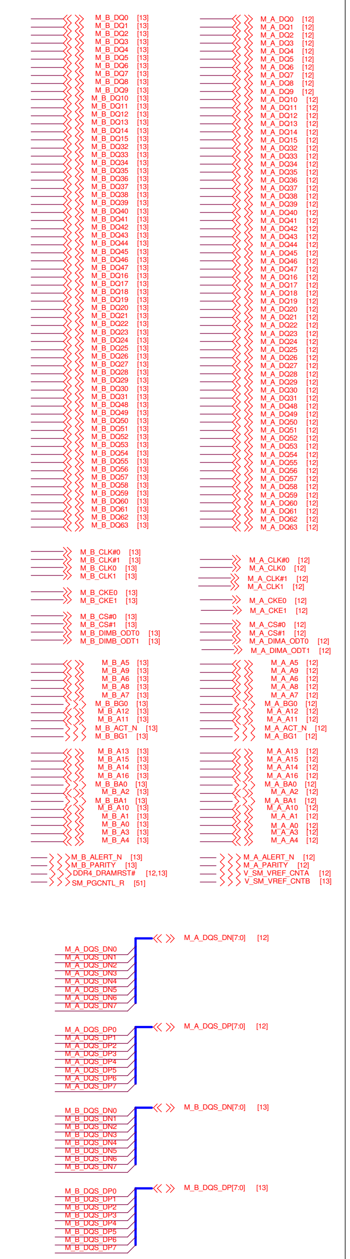
Title: CPU (DDI/EDP/TBT/TPC/)

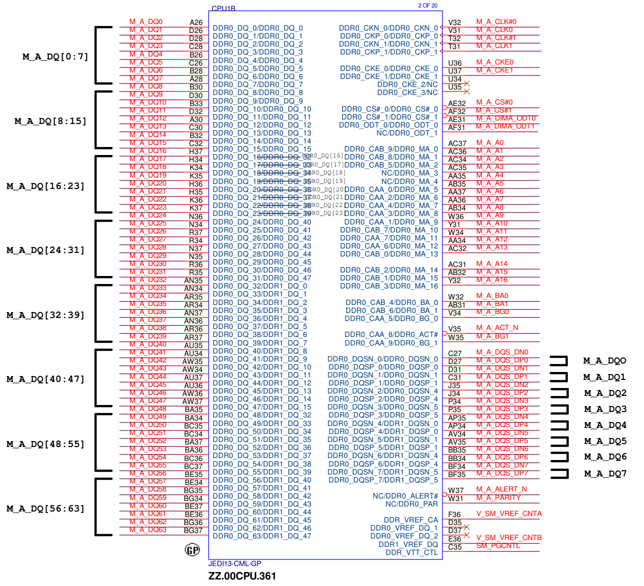
Size: A2 | Document Number: Mockingbird CML | Rev: SC

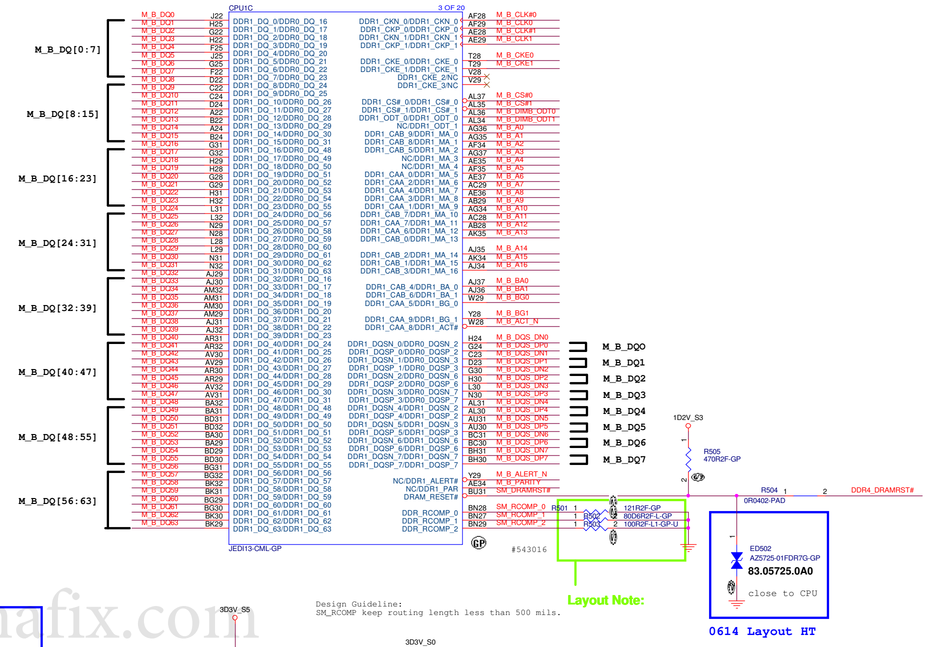
Date: Monday, December 09, 2019 | Sheet 4 of 106

Main Func = CPU

DDR4 ball type: Interleaved Type

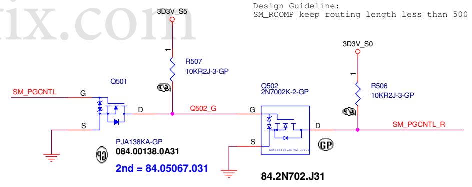






DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT



4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

<Core Design>

DELL | Wistron Corporation
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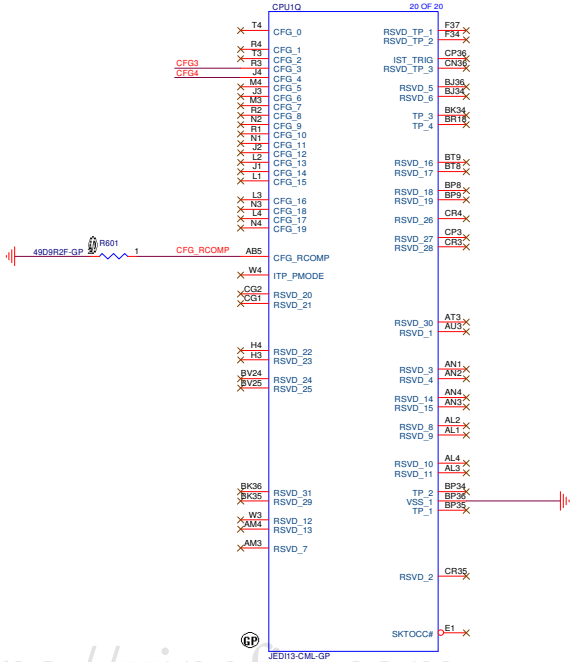
Title: CPU_(DDR)
Size: Custom | Document Number: Mockingbird CML | Rev: SC
Date: Monday, December 09, 2019 | Sheet 5 of 106

SSID = CPU

[15] CFG3
[15] CFG4



SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Design>

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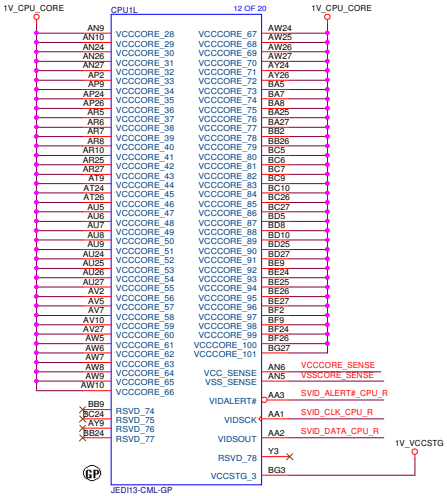
Title: CPU (CFG/IST)
Size: A2 | Document Number: Mockingbird CML | Rev: SC
Date: Monday, December 09, 2019 | Sheet 6 of 106

SSID = CPU

[46] VCCCORE_SENSE
[46] VSSCORE_SENSE

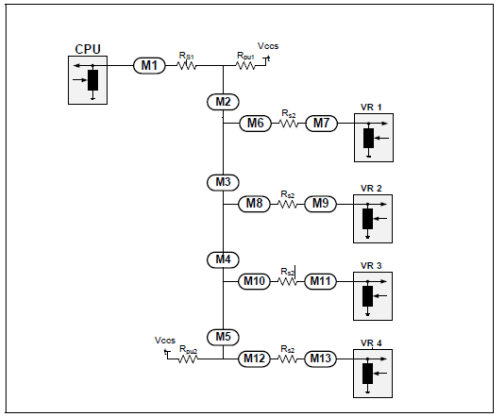
[46] SVID_DATA_CPU
[46] SVID_CLK_CPU
[46] SVID_ALERT#_CPU



Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS		76	76	2992.13	2992.13

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#						
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω						
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω						
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω						
Platform resistors tolerances	± 5%						
Route ordering	When routing at minimum spacing route Alert between Data and Clock						
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK	± 100mils						

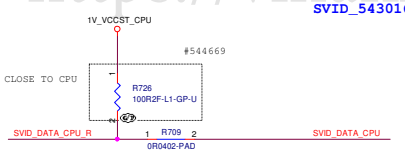
. Routing Illustration for SVID Topology



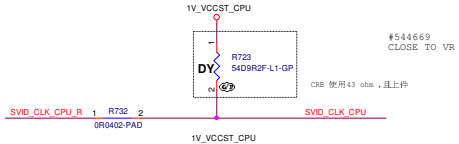
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:

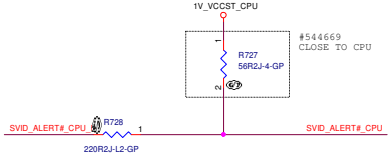
SVID DATA

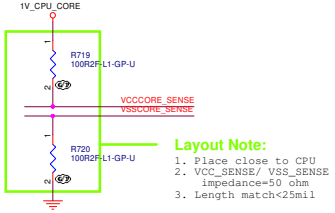


SVID CLOCK



SVID ALERT





Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

<Core Design>

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Title: CPU (VCCIN/VID)

Size: A2 | Document Number: Mockingbird CML | Rev: SC

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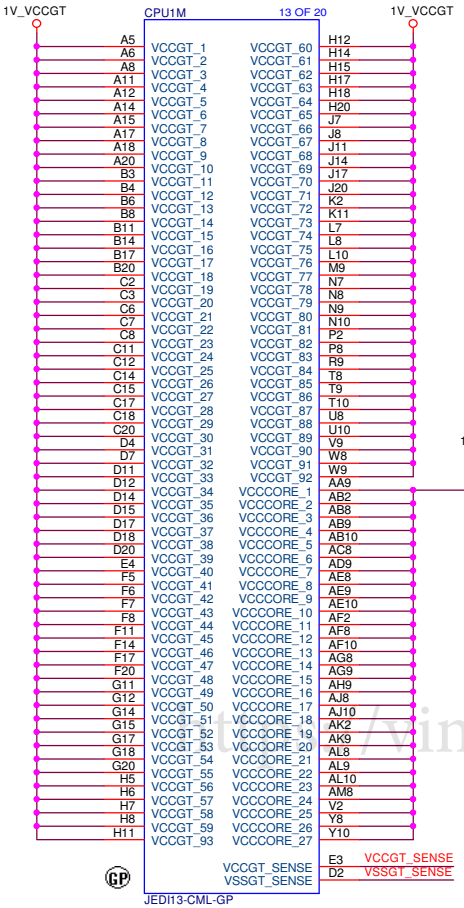
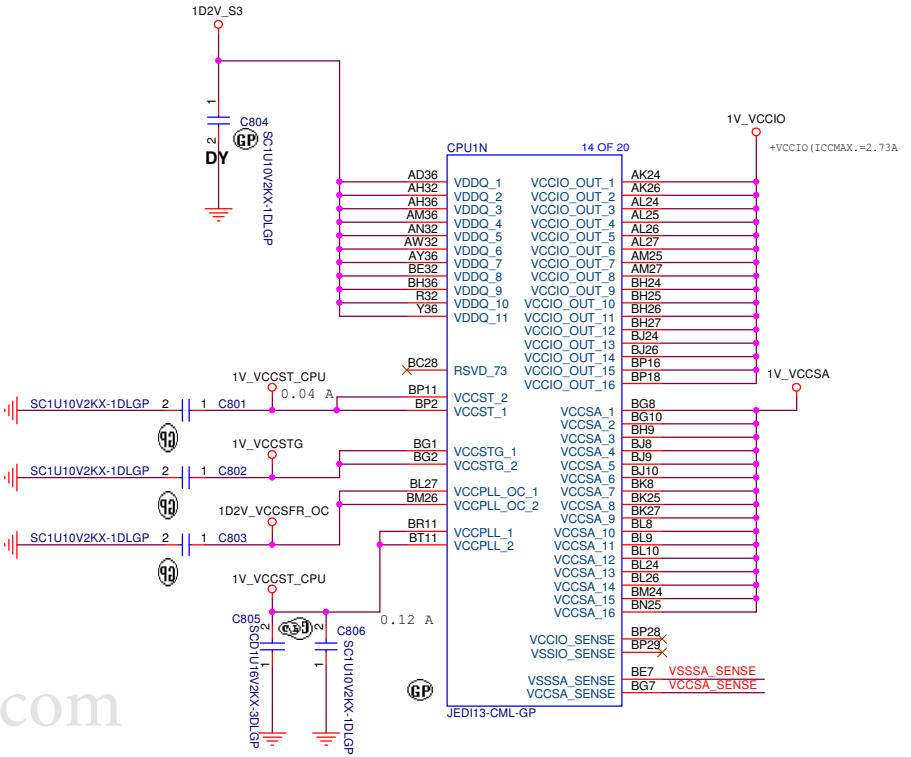
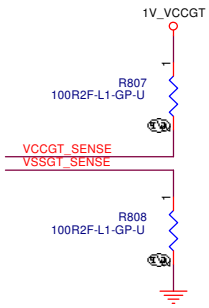
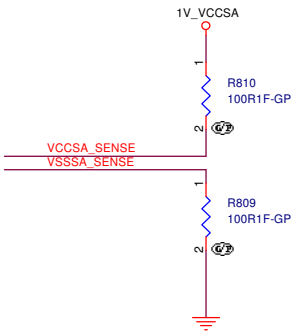
[46] VSSSA_SENSE
[46] VCCSA_SENSE
[46] VCCGT_SENSE
[46] VSSGT_SENSE

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE









<Core Design>

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Title: CPU (VDDQ/VCC/VCCST/VCCSTG)

Size: A3 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 8 of 106

Main Func = CPU

(Blanking)

<Core Design>

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Title: CPU (RSVD)

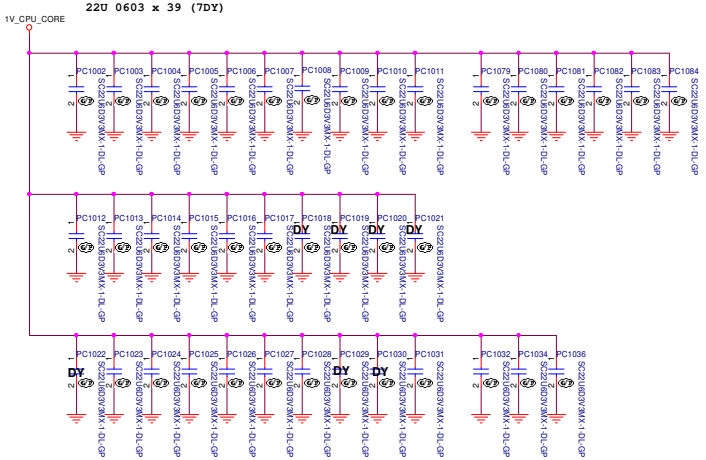
Size: A3 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 9 of 106

SSID = CPU

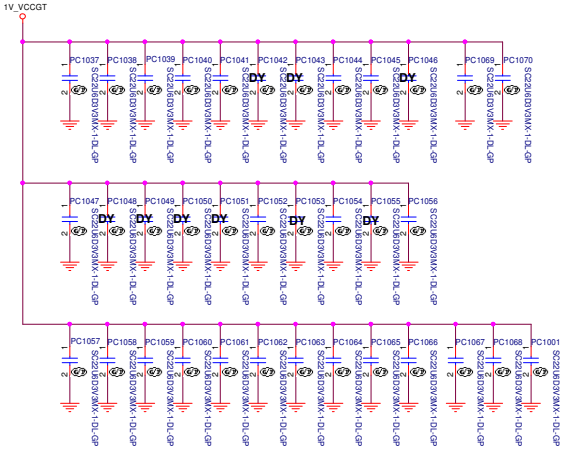
1V_CPU_CORE

22U 0603 x 39 (7DY)



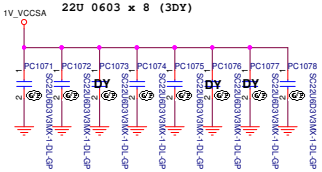
VCCGT

22U 0603 x 35 (9 DY)



VCCSA

22U 0603 x 8 (3DY)



Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
V_{CCCORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
V_{CCGT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
V_{CCCORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
V_{CCGT}	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
V_{CCSA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
V_{CCIO}	4x 1uF 0201		Place underneath the package
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
V_{CCPLL_OC}	1x 1uF 0402		Do not merge V_{CCPLL}, V_{CCPLL_OC} and V_{CCST} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
V_{CCPLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
V_{CCST}	1x 1uF 0402		
V_{CCSTG}	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU(CORE Power Cap1)*

Size: A2 | Document Number: *Mockingbird CML* | Rev: *SC*

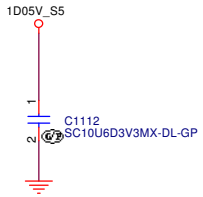
Date: Monday, December 09, 2019 | Sheet 10 of 106

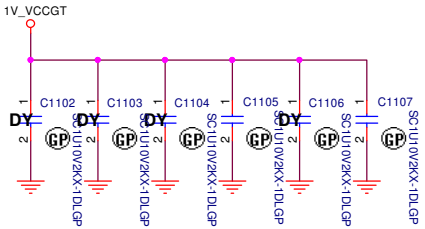
SSID = CPU

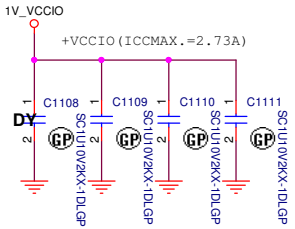
PCH DERIVED RAILS

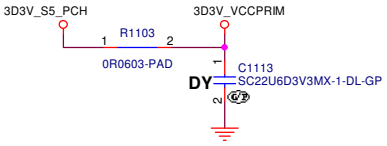
UNSLICED GT

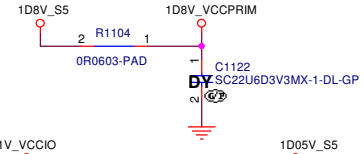
VCCIO

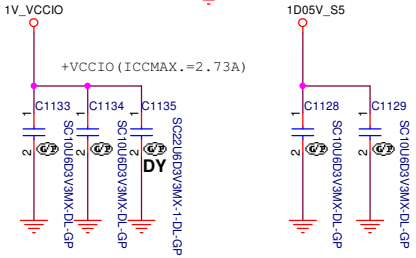


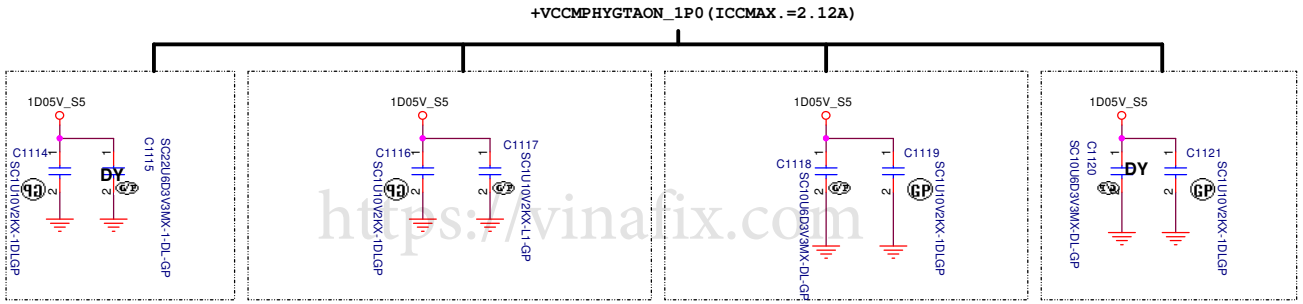






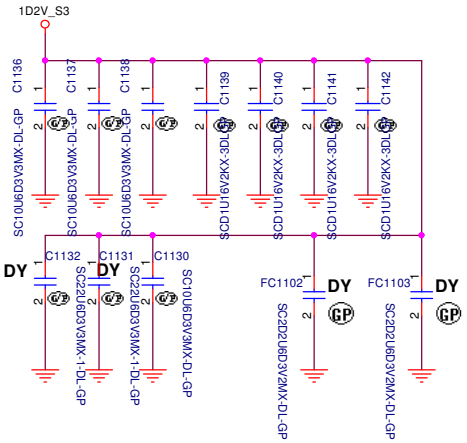


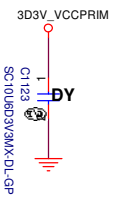




Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15





U-line 23e 28W
IccMax current-10ms max = 34 A

<Core Design>

Wistron Corporation
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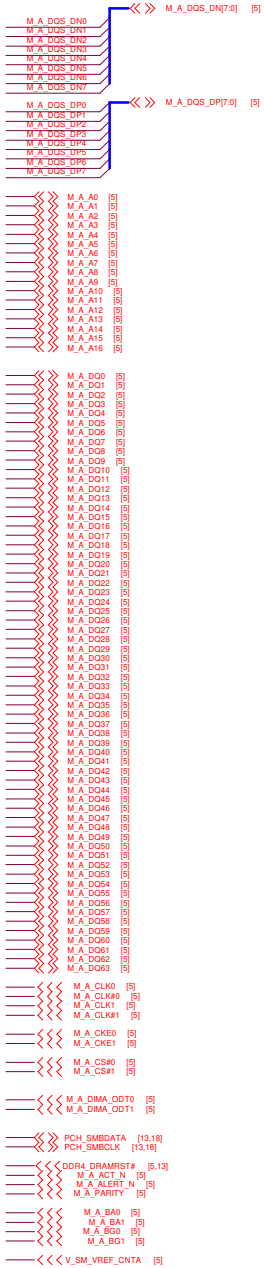
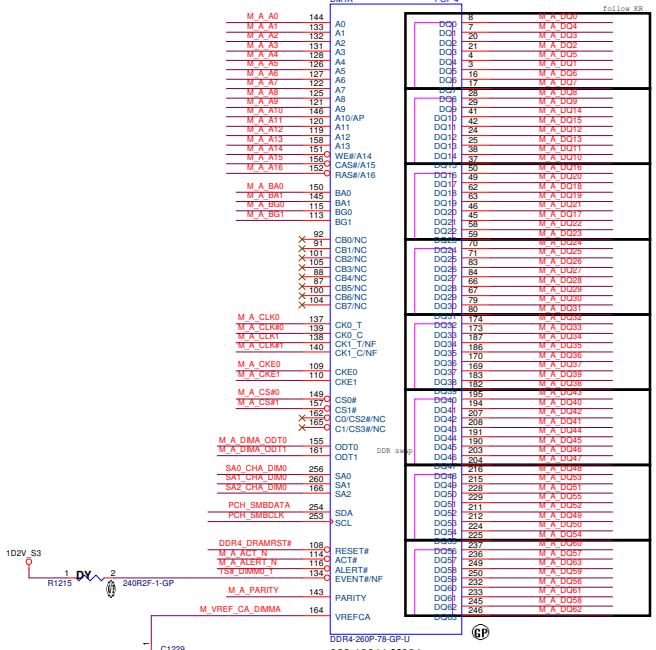
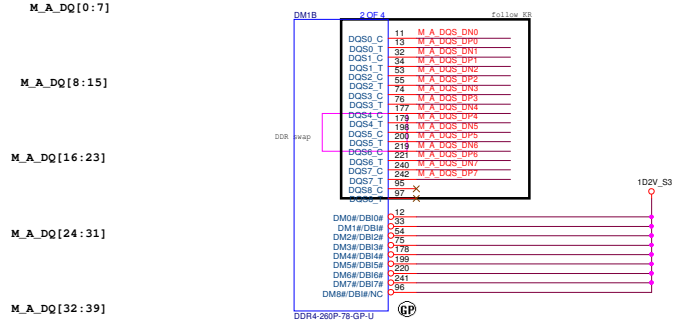
Taipei Hsien 221, Taiwan, R.O.C.

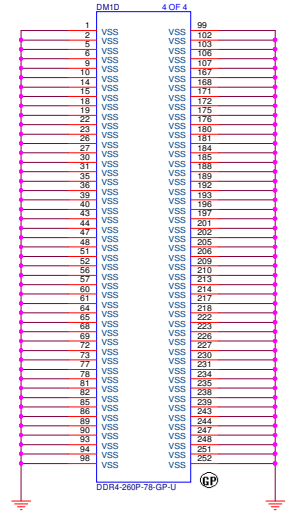
Title	CPU_(Power CAP2)	
Size: A3	Document Number: Mockingbird CML	Rev: SC
Date: Monday, December 09, 2019	Sheet 11 of 106	

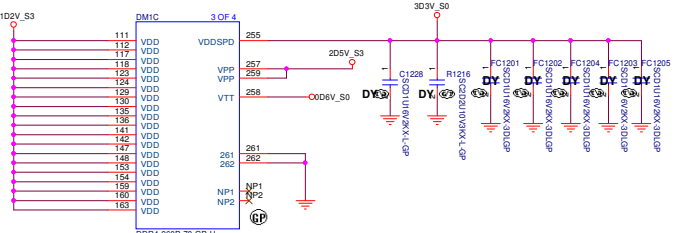
Main Func = MEMORY

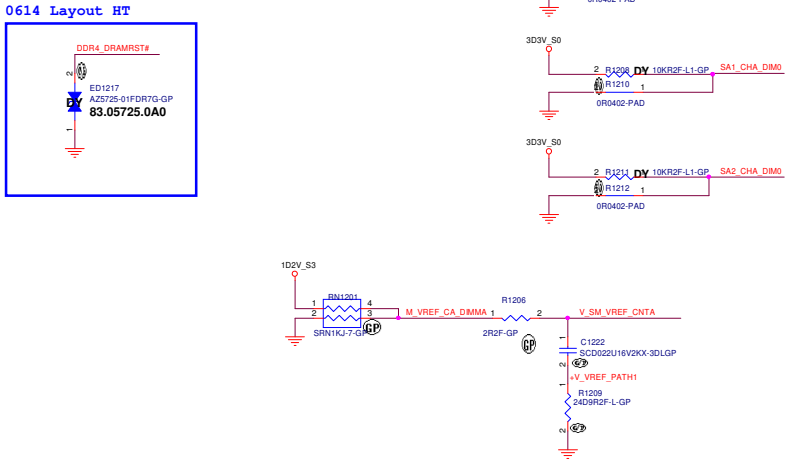


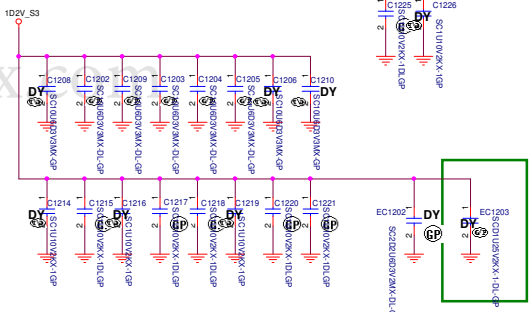


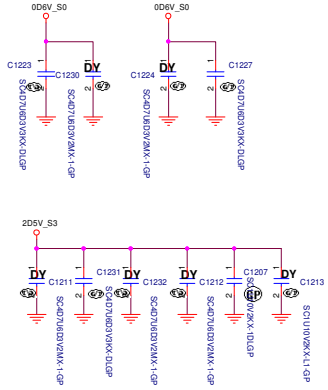






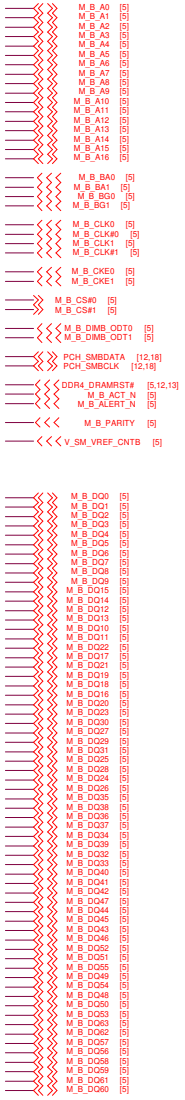


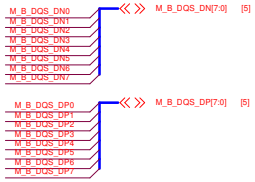


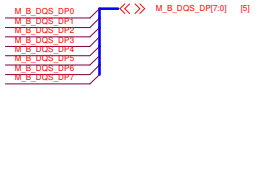


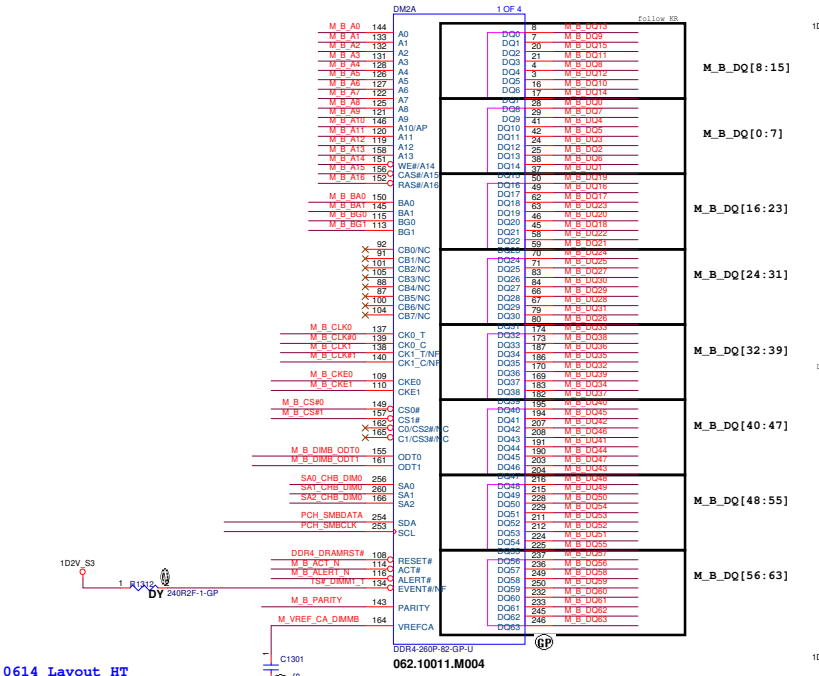
0614 Layout HT

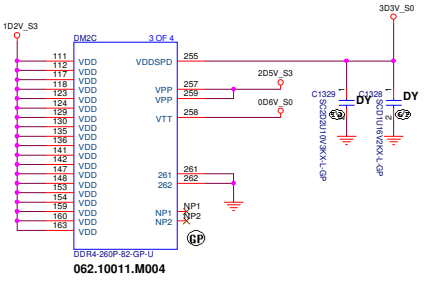
Main Func
= MEMORY

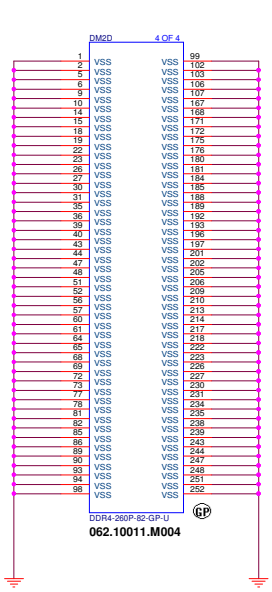


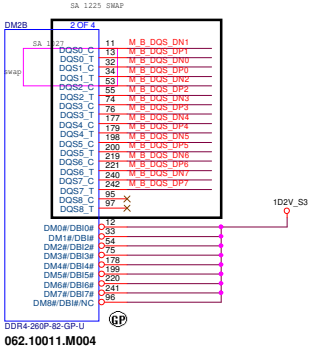


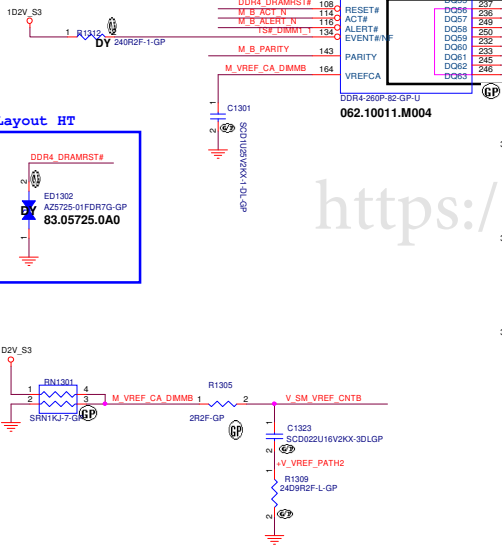


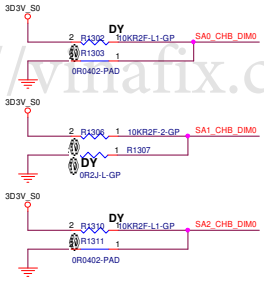




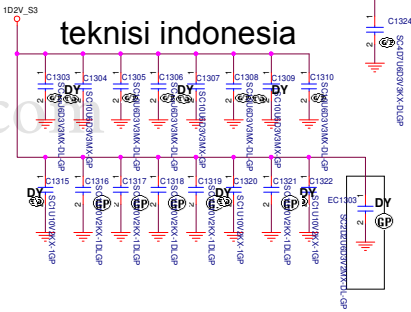


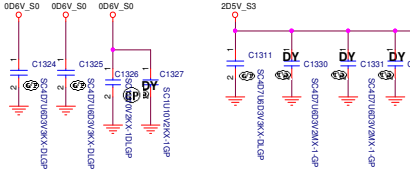






0614 Layout HT





teknisi indonesia

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 13 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
DDR (RSVD) (DDR4-CHA1)

Size	Document Number	Rev
A4	Mockingbird CML	SC

Date: Monday, December 09, 2019 Sheet 14 of 106

Main Func = PCH

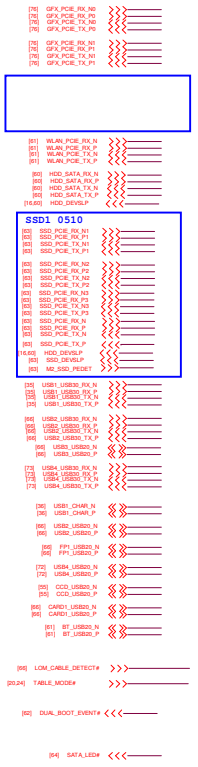
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address bit to select the "other" half of the BIOS. The processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert the A16 (Boot), the A17 (Descriptor), or the A18 (Integrated GbE) bit of the value going to the top of the address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. Top Swap Boot Block is configurable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 0). Bit 0 — Boot BIOS Destination 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or descriptor override configuration will not affect SPI accesses initiated by Intel ME or Integrated GBE LAN. 4. This signal is in the primary well.
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

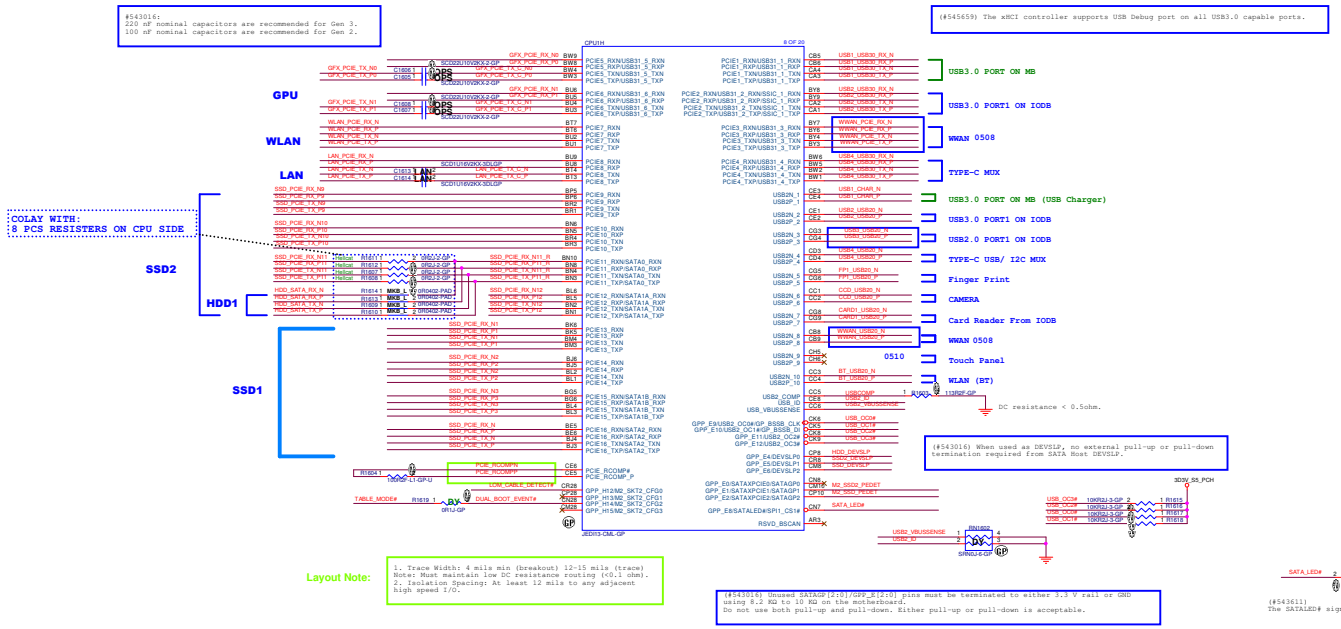
PCH strap pin:

Vinafix.com

Wistron Corporation
CPU (STRAP)
Mockingbird CRB

Main Func = PCH





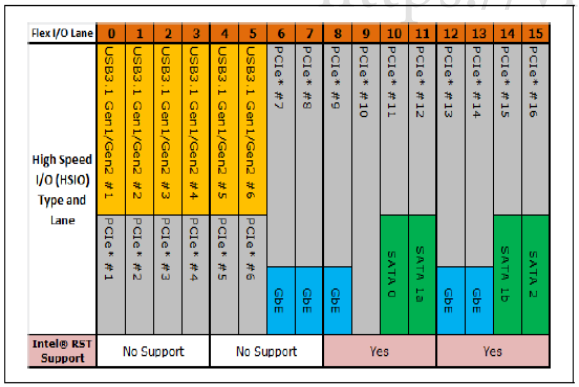


Table 1-3. PCH HSIO Detail

SKU	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Mainstream/ Base-U	USB 3.1 Gen 1	USB 3.1 Gen 1	USB 3.1 Gen 1	USB 3.1 Gen 1	PCIe*	PCIe*	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	SATA 0/ PCIe*	SATA 1A/ PCIe*	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*	PCIe*
Premium-U	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*/ SATA 1B	PCIe*/ SATA 2
Premium-Y	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	PCIe*/ USB 3.1 Gen 1/ Gen 2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	Not Available	Not Available

Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
										Cycle Router #2				Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP6	RP7	RP5		RP12	RP11	RP9		RP15	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

	BOOKY	Rogue
USB_OC0#	TYPEC PD	NC
USB_OC1#	Power share	USB3.0 Power
USB_OC2#	USB3.0 Power	NC
USB_OC3#	USB2.0 Power	TYPEC PD

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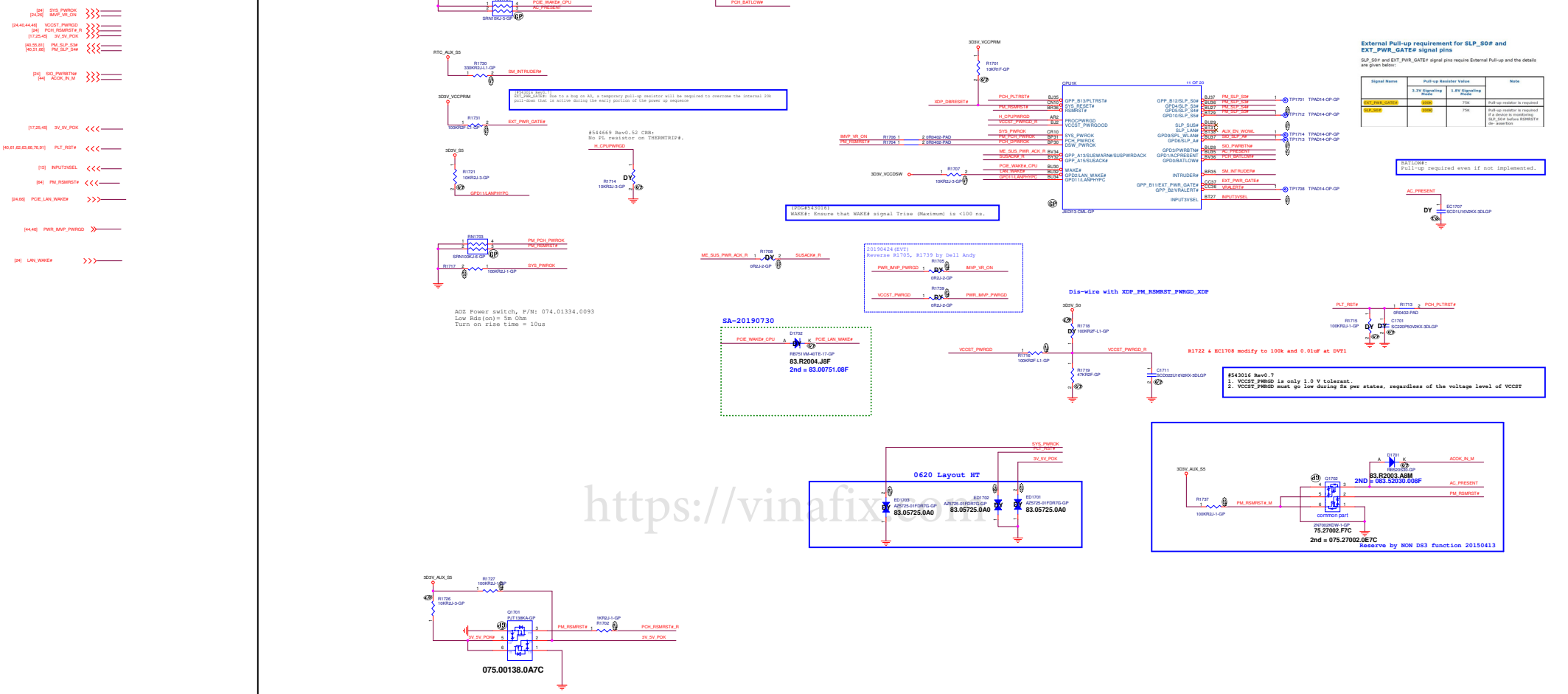
CPU (PCIE/SATA/USB)

Mockingbird CML

SC

SSID = PCH



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

PCH_(PMU)

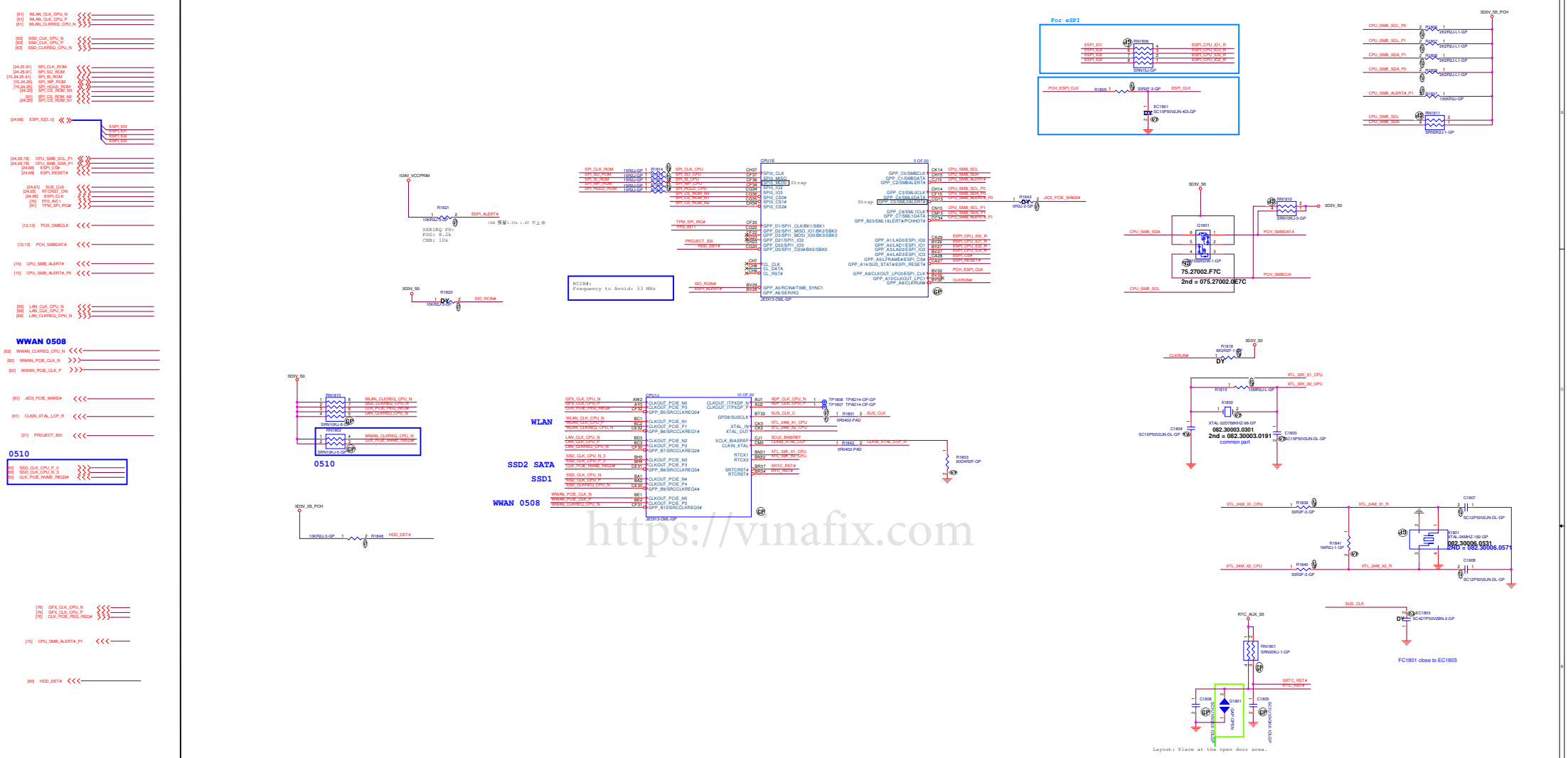
Size: A1 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 17 of 186

SSID = PCH

WWAN 0508

0510



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

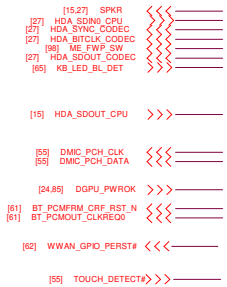
CPU (SPI/ESPI/SMBS/XTAL/CLK)

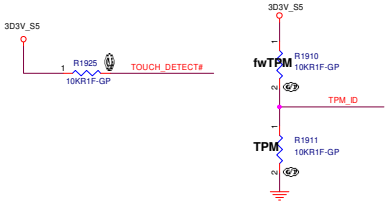
Mockingbird CML

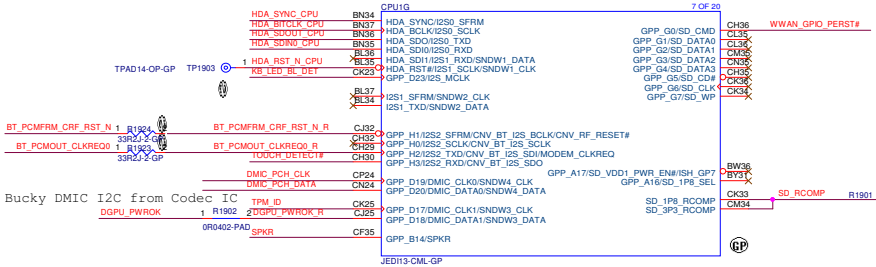
SC

Monday, December 09, 2019

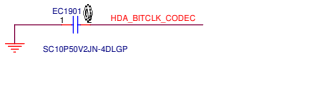
SSID = PCH



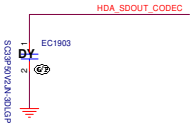




Bucky DMIC I2C from Codec IC



R1920~R1921 need to close for merge prepare



<Core Design>

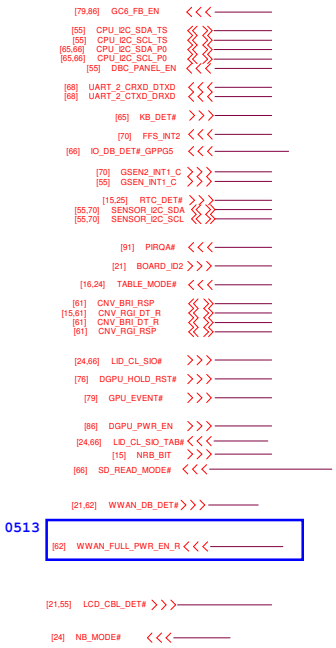
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

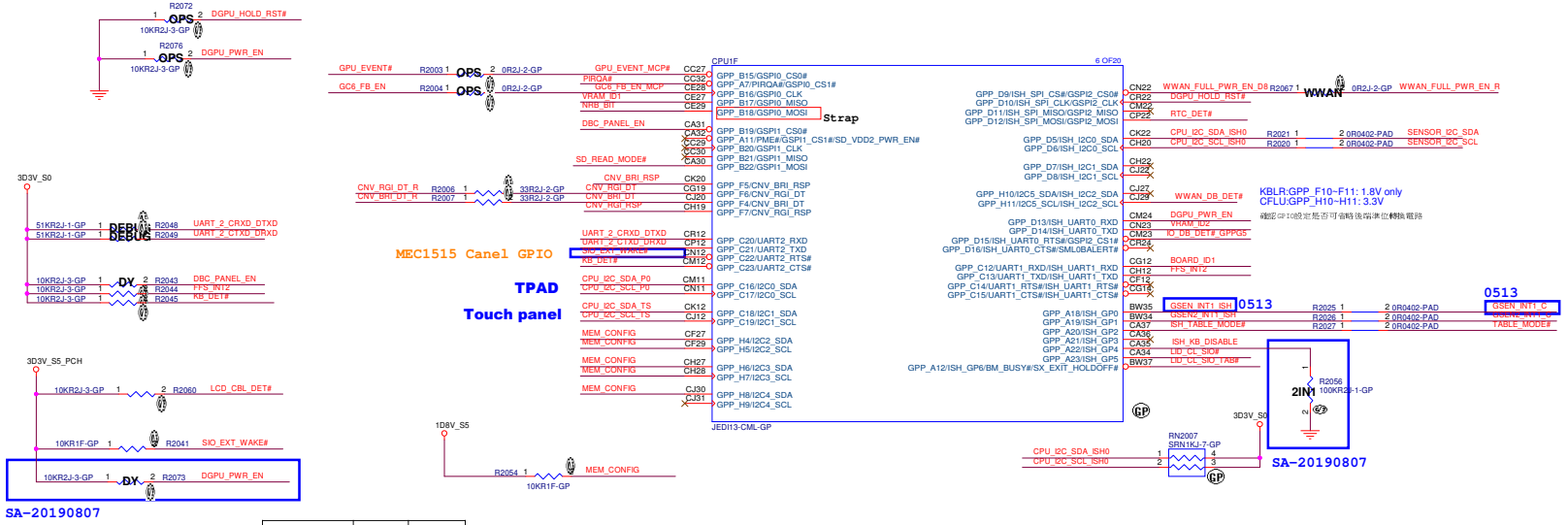
Title: CPU (HAD/I2S/SD/DMIC)

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 19 of 106

SSID = PCH

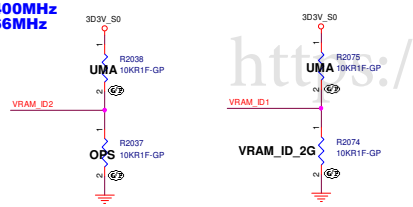


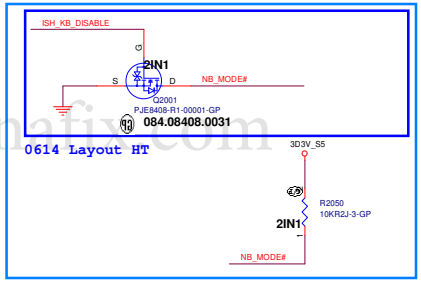


	H(10K)	L(10K)
VRAM_ID2	UMA	OPS
BOARD_ID2	2IN1	CLAM
BOARD_ID1	CNL	WHL-U
NB_MODE#	2IN1	CLAM

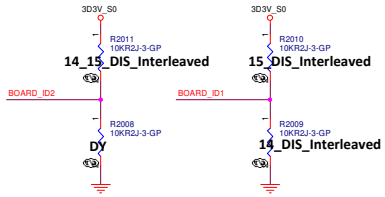
(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

UMA: 2400MHz
DIS: 2666MHz





	NB_MODE	LID_CL_SIO_TAB#	
NB Mode	1	1	KB可以動
Tablet Mode	don´t care	0	KB鎖住
ClamShell Mode	0	1	KB鎖住



BOARD_ID[2:1]	Board SKU ID	11	15 DIS interleaved
		10	14 DIS interleaved
		01	15 UMA non interleaved
		00	14 UMA non interleaved

<Core Design>

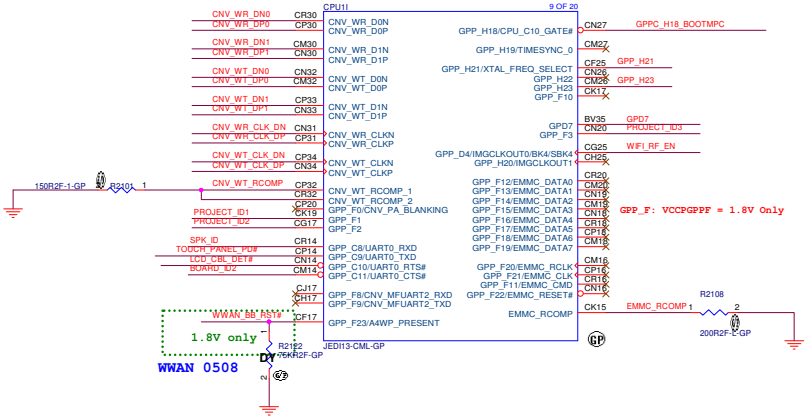
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

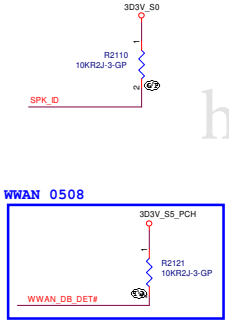
Title: CPU (UART/I2C/ISH)
Size: A2 | Document Number: Mockingbird CML | Rev: SC
Date: Monday, December 09, 2019 | Sheet 20 of 106

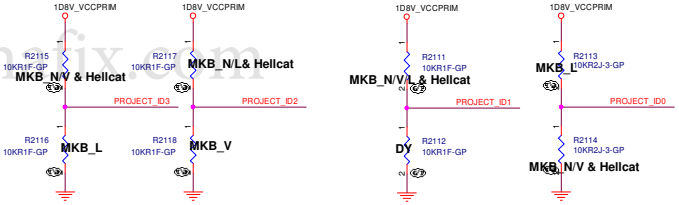
SSID = PCH

SSID = PCH

[40] GPPC_H18_BOOTMPC
[61] WIFI_RF_EN
[20] BOARD_ID2
[15] GPP_H23
[15] GPP_H21
[61] CNV_WT_CLK_DN
[61] CNV_WT_CLK_DP
[61] CNV_WT_DP0
[61] CNV_WT_DN0
[61] CNV_WT_DP1
[61] CNV_WT_DN1
[61] CNV_WR_CLK_DN
[61] CNV_WR_CLK_DP
[61] CNV_WR_DP0
[61] CNV_WR_DN0
[61] CNV_WR_DP1
[61] CNV_WR_DN1
[18] PROJECT_ID0
[15] GPD7
[62] WWAN_BB_RST#
[20,62] WWAN_DB_DET#
[20,55] LCD_CBL_DET#
[29] SPK_ID
[55] TOUCH_PANEL_PD#







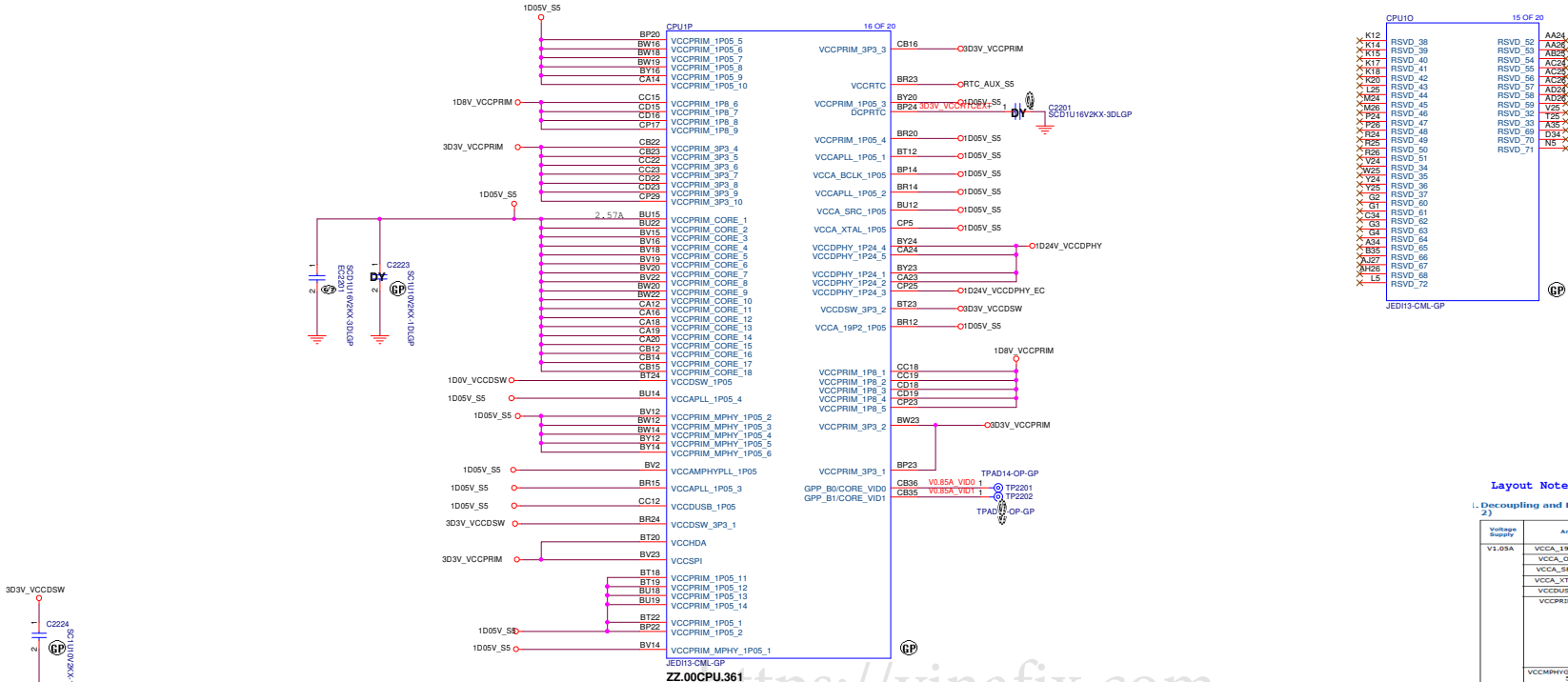
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude (Reseved)
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Sereis
		10	5000 Series
		01	7000 Series
		00	N/A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVI)
Size: A2
Document Number: Mockingbird CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 21 of 106

SSID = PCH



Layout Note:

1. Decoupling and Power Connection Requirements for WHL U PCH (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.05A	VCCA_19P2_1P05	BR12	-	-	-	-	-
	VCCA_OC_1P05	BP14	-	-	-	-	-
	VCCA_SRC_1P05	BU12	-	-	-	-	-
	VCCA_XTAL_1P05	CP5	1uF	0402	1	E	CP5
	VCCDUSB_1P05	CC12	-	-	-	-	
	VCCPRIM_1P05	BT12, BR14, BR15, BU14, BT22, BP20, BW16, BW18, BW19, BV16, CA14, BR20, BY20, BT18, BT19, BU18, BU19	1uF	0402	1	E	BP20
	VCCMPHYGTAON_1P05	BV12, BW12, BW14, BV12, BV14, BV14	22uF	0603	1	E	BV12
	VCCAMPHYPLL_1P05	BV2	1uF	0402	1	E	BV2
V1.0A / V0.85A	VCCPRIM_CORE	BU15, BU22, BV13, BV16, BV18, BV19, BV20, BV22, BW20, BW22, CA12, CA16, CA18, CA19, CA20, CB12, CB14, CB15	1uF	0402	1	E	BV18, Note 1
V1.8A	VCCPRIM_1P8	CC18, CC19, CD18, CD19, CP23,CC15, CD15, CD16, CP17	1uF	0402	1	E	CP17
			1uF	0402	1	E	CP23, Note 1

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V3.3A	VCCPRIM_3P3	CB22, CB23, CC22, CC23, CD22, CD23, CP29,BW23, BP23, CB16	0.1uF	0402	1	E	CP29, Note 1
			1uF	0402	1	E	CP29, Note 1
V3.3A/ V1.8A	VCCSPI	BV23	-	-	-	-	-
V3.3A/ V1.5A/ V1.8A	VCCHDA	BT20	-	-	-	-	-
V3.3DSW	VCCDSW_GPIO	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1		
PCH Internal VRM	VCCDSW_1P05	BT24	1uF	0402	1	E	BT24
	VCCRTCEXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_1P24	BY23, CA23, CP25, BY24, CA24	4.7uF	0402	1	E	CP25

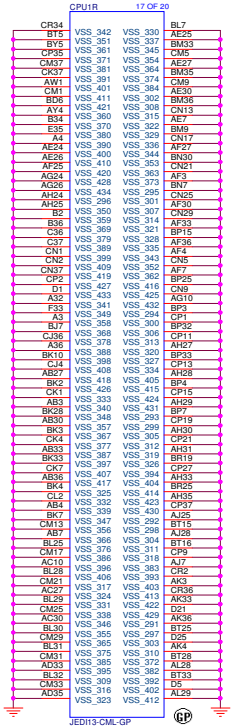
Notes:
1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of (R)unway, and (E)dge decoupling capacitor placement, refer to "Loop Inductance Reduction Decoupling".
5. Refer to Electromagnetic Interference chapter for recommended placement
6. Refer to the vendor requirements for bulk decoupling which will be in addition to the recommendation mentioned in the table above.

<Core Design>

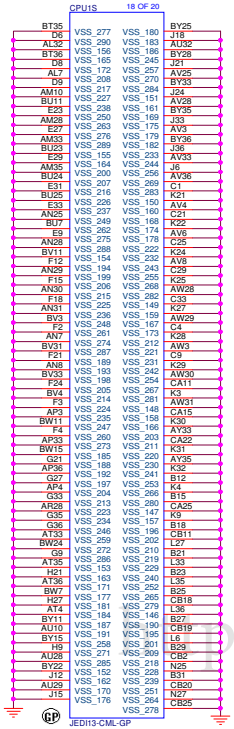
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)
Size: A2 | Document Number: Mockingbird CML | Rev: SC
Date: Monday, December 09, 2019 | Sheet 22 of 106

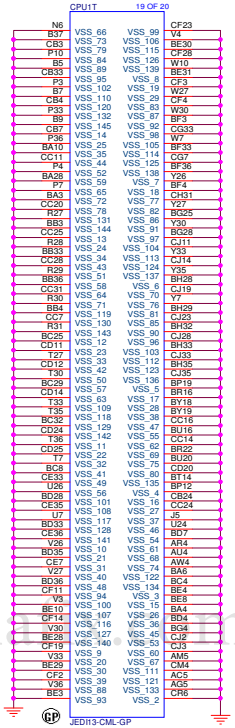
SSID = PCH



ZZ.00CPU.361



ZZ.00CPU.361



ZZ.00CPU.361

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

Wistron Corporation
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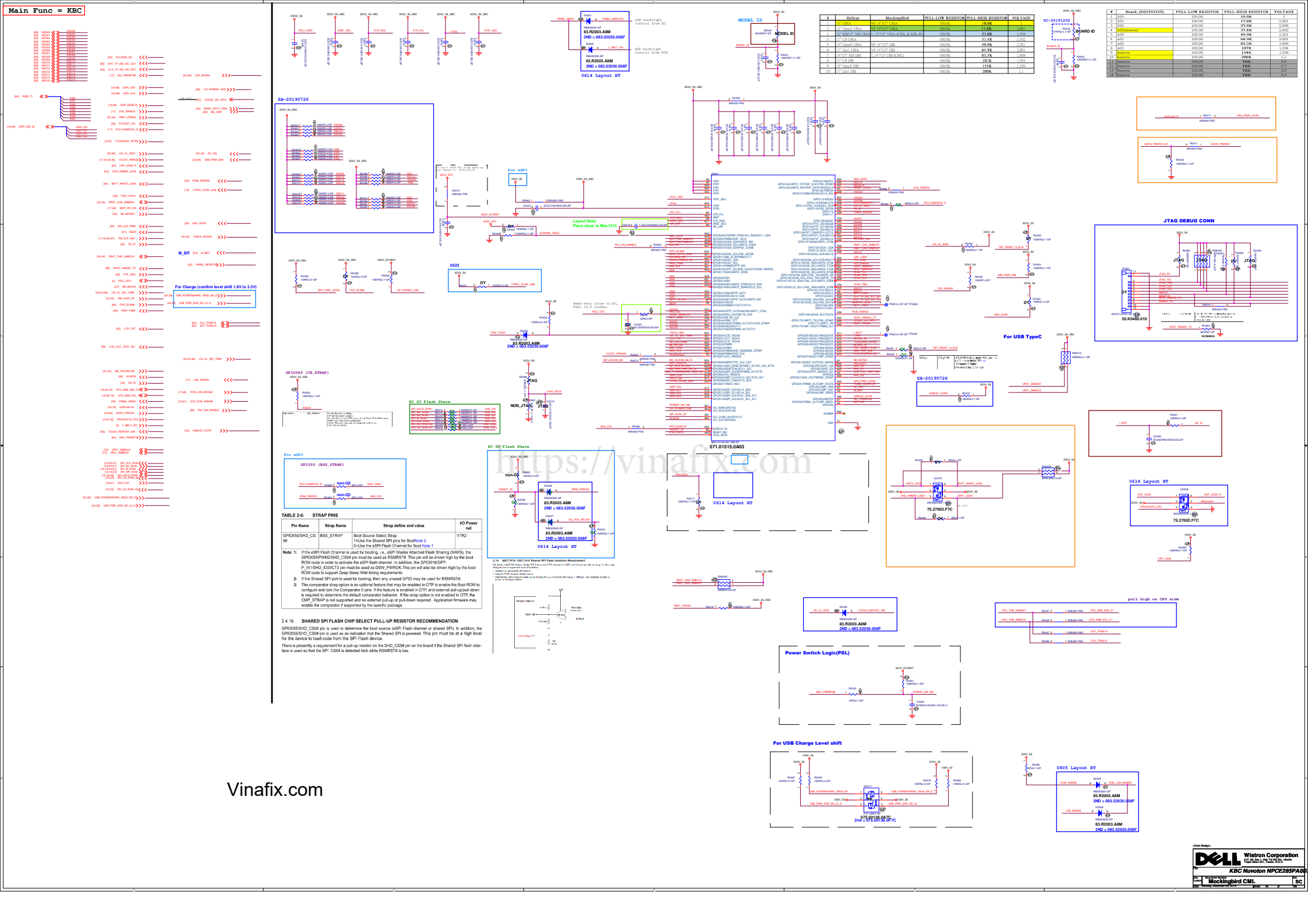
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(VSS)

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 23 of 106



Hellcat	MockingBird	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	14" UMA	N5 14"/15" UMA	10.0K	3
2	14" Unqui UMA	V5 14"/15" UMA	17.8K	2.801
3	15" N5S/7 MS UMA	14"/15" UMA (CMI & KBL-R)	27.0K	2.496
4	14" CS UMA		37.4K	2.402
5	15" Unqui UMA	N5 14"/15" DIS	49.9K	2.201
6	15" 2in1 UMA	V5 14"/15" DIS	64.9K	2.001
7	14"/15" N5 DIS		82.5K	1.806
8	17" CS DIS		107K	1.594
9	15" Unqui DIS		154K	1.299
10	17" 2in1 DIS		200K	1.1

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(Reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot Note 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/CT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI_CS0# is detected high while RSMRST# is low.

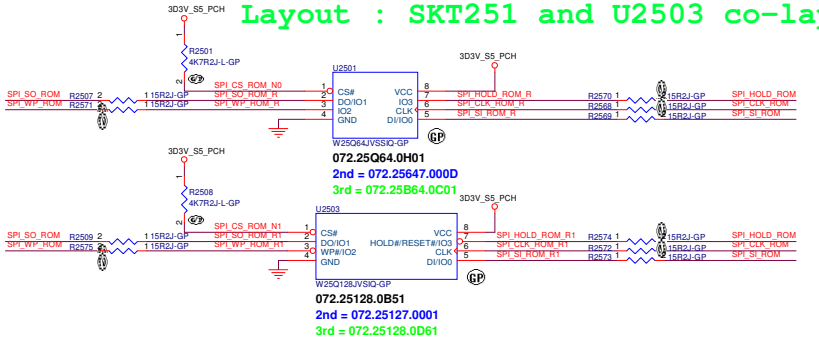
Main Func = SPI Flash

Socket for 16M

SPI Flash ROM1(8M)+ROM2(16MB) for PCH

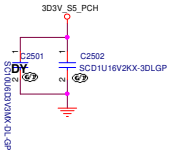
Layout : SKT251 and U2503 co-lay

[18,24] SPI_CS_ROM_N1
[18,24] SPI_CS_ROM_N0
[18,24,91] SPI_SO_ROM
[18,24,91] SPI_CLK_ROM
[15,18,24,91] SPI_SI_ROM
[15,18,24] SPI_HOLD_ROM
[15,18,24] SPI_WP_ROM



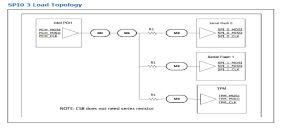
072.25Q64.0H01
2nd = 072.25647.000D
3rd = 072.25B64.0C01

072.25128.0B51
2nd = 072.25127.0001
3rd = 072.25128.0D61



Dual SPI0 Devices + TPM Topology Guidelines

The CFL PCH supports TPM through SPI0 bus. The topology below was a full configuration which consist of 2 SPI0 Flash and 1 TPM device. The system can be configured with 1 SPI0 Flash and 1 TPM device.

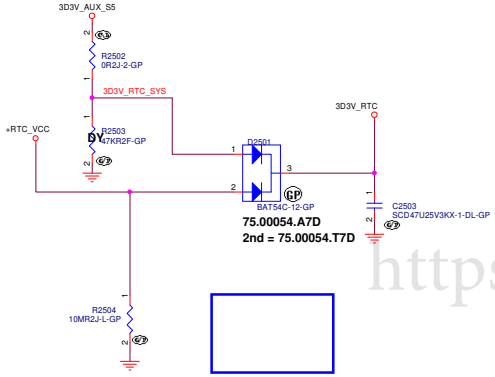


Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, mils	
				Segment	Total	Segment	Total

Notes:
1. R1 Resistor should be 15 ohm for 1.8V and 33 ohm for 3.3V. SPI0_IO2 and SPI0_IO3 connection to be pulled up with 1k ohm on R2 resistor.
2. 5 number of vias can be allowed.
3. Reference plane should be Continuous Ground Plane only allowed.
4. This topology relates to SPI0_IO_2 to 3, SPI0_MOSI, SPI0_MISO and SPI0_CLK
5. Design guideline support up to 50MHz.

Main Func = RTC

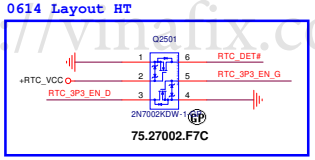
[15,20] RTC_DET#
[24] VCCDSW_EN
[24] RTCRST_ON



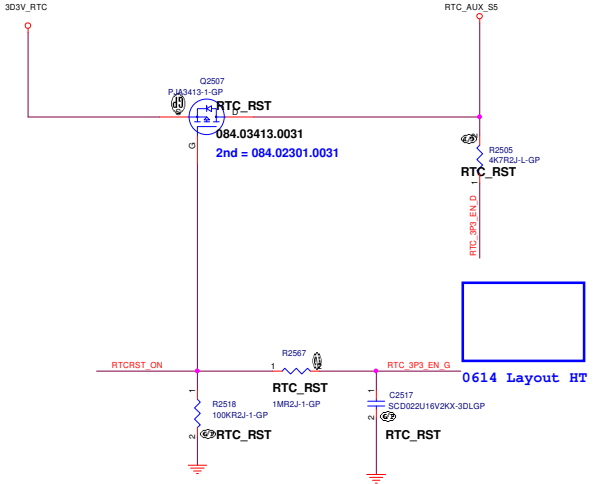
75.00054.A7D
2nd = 75.00054.T7D

0614 Layout HT

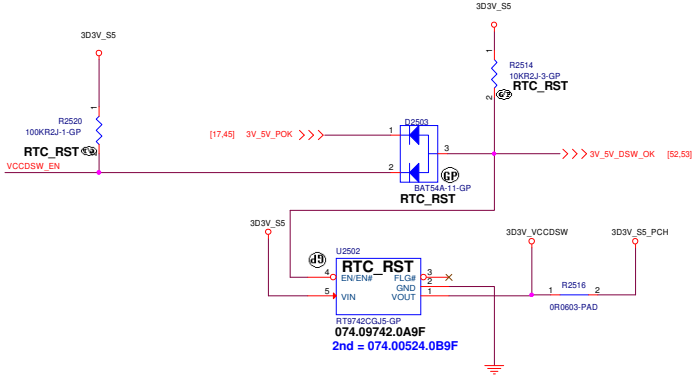
0614 Layout HT



75.27002.F7C



0614 Layout HT



074.09742.0A9F
2nd = 074.00524.0B9F

<Core Design>

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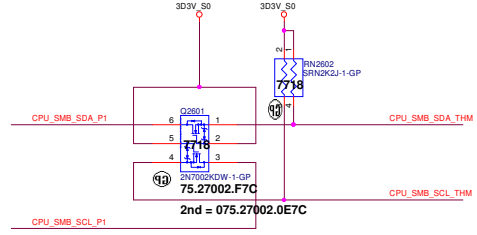
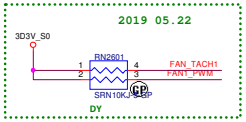
Title: Flash
Size: A2
Document Number: Mockingbird CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 25 of 106

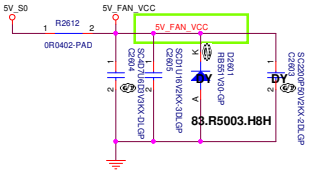
Main Func = Thermal Sensor

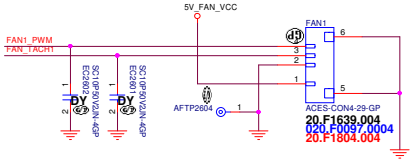
PWM FAN1

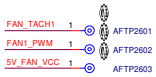
Layout Note:
Signal Routing Guideline:
Trace width = 15mil



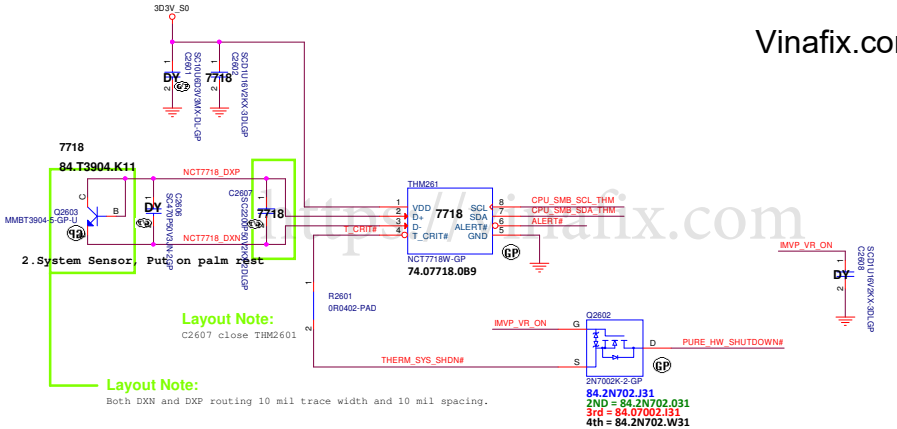








[18,24,79] CPU_SMB_SDA_P1
[18,24,79] CPU_SMB_SCL_P1
[17,24] IMVP_VR_ON
[40] PURE_HW_SHUTDOWN#
[24] FAN1_PWM
[24] FAN_TACH1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<Core Design>

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Title: THERMAL NCT7718W/Fan
Size: A2
Document Number: Mockingbird CML
Rev: SC
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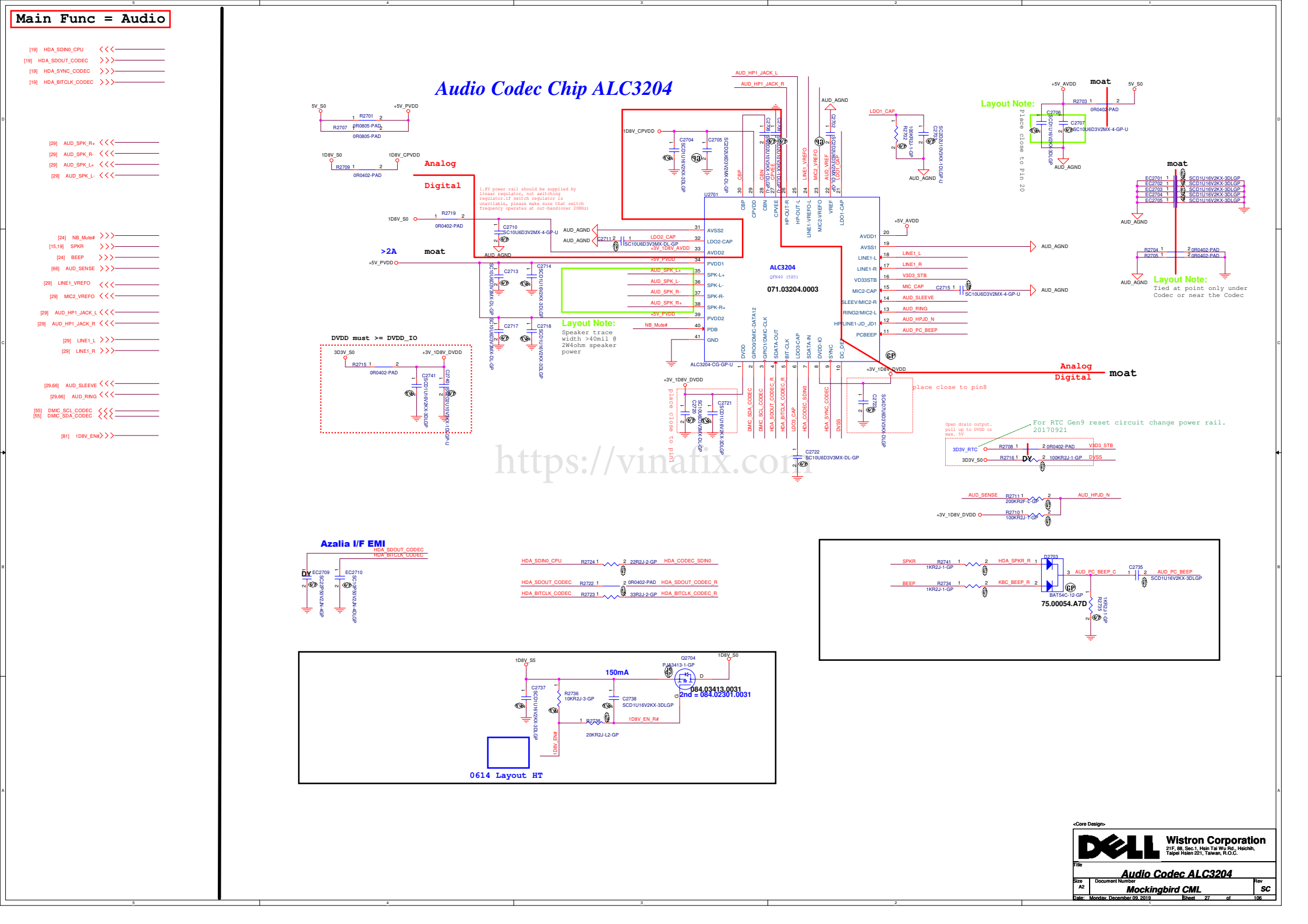
Main Func = Audio



(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	*Mockingbird CML*	*SC*

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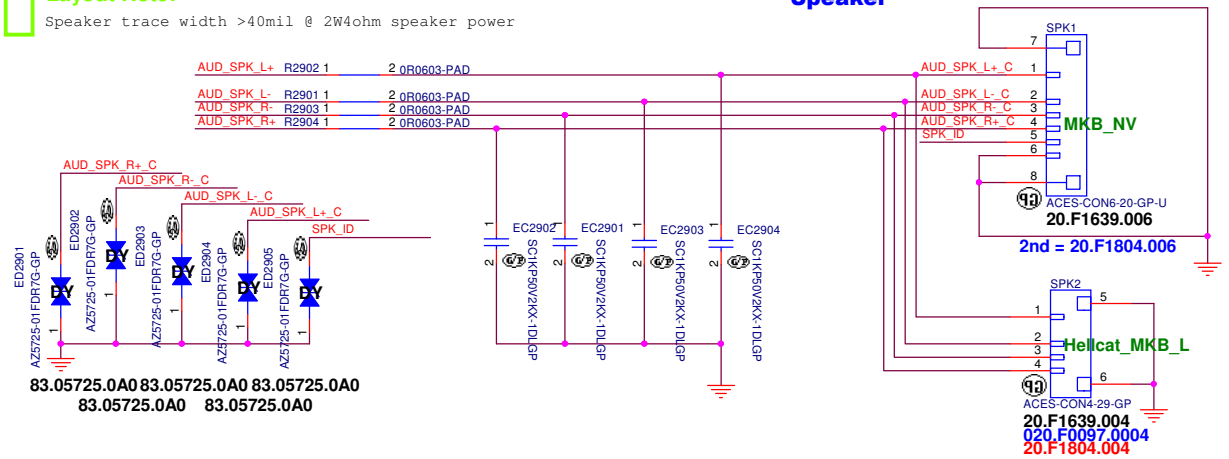
Main Func = Audio

[27] AUD_SPK_R+
[27] AUD_SPK_R-
[27] AUD_SPK_L-
[27] AUD_SPK_L+

[21] SPK_ID

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

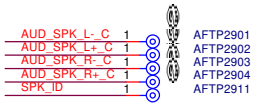
Speaker



83.05725.0A0 83.05725.0A0 83.05725.0A0
83.05725.0A0 83.05725.0A0

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID Short: 2514
Un-connect: 3209



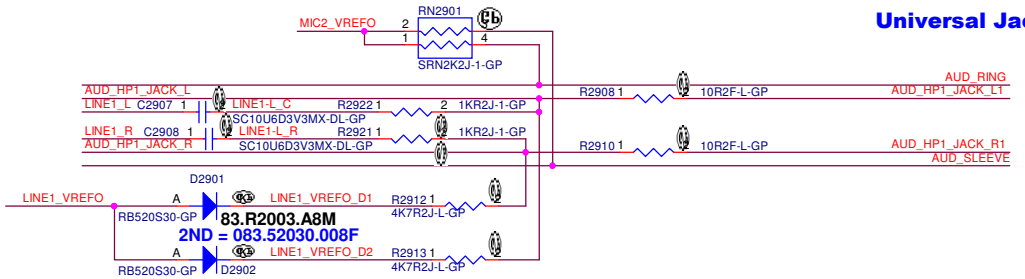
From Codec

[27] MIC2_VREFO
[27,29,66] AUD_RING
[27] AUD_HP1_JACK_L
[27] LINE1_L
[27] LINE1_R
[27] AUD_HP1_JACK_R
[27,29,66] AUD_SLEEVE
[27] LINE1_VREFO

To IO Board

[27,29,66] AUD_RING
[66] AUD_HP1_JACK_L1
[66] AUD_HP1_JACK_R1
[27,29,66] AUD_SLEEVE

Universal Jack (Moved to I/O Board)



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Title: **Audio IO**

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A3	Mockingbird CML	SC

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Title *(Reserved)*		
Size A4	Document Number Mockingbird CML	Rev SC
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Main Func = LAN

<Core Design>

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Title
LAN RTL8106

Size	Document Number	Rev
Custom	Mockingbird CML	SC

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Main Func = LAN

<Core Design>

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Title: XFOM&RJ45

Size: A3 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 32 of 106

Main Func = Card Reader

<Core Design>

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Title

Card Reader-RTS5170

Size	Document Number	Rev
A4	Mockingbird CML	SC

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Main Func = USB2.0

<Core Design>

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Title: USB2.0 CONN

Size | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 34 of 106

Main Func = USB3.0 Port1

[24,66] USB_PWR_EN#

[16,36] USB_OC2#

[36] USB1_USB20_N
[36] USB1_USB20_P

[16] USB1_USB30_TX_N
[16] USB1_USB30_TX_P
[16] USB1_USB30_RX_N
[16] USB1_USB30_RX_P

5V_USB30_VCCA

U3502 **2A**

VOUT VIN
GND
OCB EN#

USB_OC2# USB_PWR_EN# (Active Low)

APL3553BBI-TRG-GP
074.03553.007G
NON_PS

5V_S5

C3507 SCD1U10V2KX-1-GP

NON_PS

0614 Layout HT

ED3502

USB1_USB20_CON_N
USB1_USB20_CON_P

AZ5315-02F-GP
83.05315.0A0

EL3501

USB1_USB20_N ↔ USB1_USB20_CON_N
USB1_USB20_P ↔ USB1_USB20_CON_P

DLM0NSN900HY2D-GP
068.09002.2001

C3512 SCD1U16V2KX-3DLGP
USB1_USB30_TX_P → USB1_USB30_TX_CMC_P → R3501 0R0402-PAD → USB1_USB30_TX_CON_P

USB1_USB30_RX_P → R3503 0R0402-PAD → USB1_USB30_RX_CON_P

C3511 SCD1U16V2KX-3DLGP
USB1_USB30_TX_N → USB1_USB30_TX_CMC_N → R3502 0R0402-PAD → USB1_USB30_TX_CON_N

USB1_USB30_RX_N → R3504 0R0402-PAD → USB1_USB30_RX_CON_N

Stuff for ESD R2 spec

ED3501

USB1_USB30_RX_CON_N ↔ USB1_USB30_RX_CON_N
USB1_USB30_RX_CON_P ↔ USB1_USB30_RX_CON_P
USB1_USB30_TX_CON_N ↔ USB1_USB30_TX_CON_N
USB1_USB30_TX_CON_P ↔ USB1_USB30_TX_CON_P

AZ1043-04F-R7G-GP
075.01043.0073

USB3.0 Port 1

Layout Note: Close USB3

5V_USB30_VCCA

2A

C3508 SCD1U16V2KX-3DLGP
C3510 SCD1U10V2KX-L1-GP
C3509 SCD1U6D3V2MX-1-DL-GP
C3506 SCD1U6D3V2MX-1-DL-GP

USB3.0 Port1

5V_USB30_VCCA

USB3

VBUS
D-
D+
GND
GND

USB1_USB20_CON_N
USB1_USB20_CON_P
USB1_USB30_RX_CON_N
USB1_USB30_RX_CON_P
USB1_USB30_TX_CON_N
USB1_USB30_TX_CON_P
STDA_SSRX-
STDA_SSRX+
STDA_SSTX-
STDA_SSTX+

SKT-USB13-513-GP
022.10005.0KF1

Main Func = USB3.0 Port2

0513

<Core Design>

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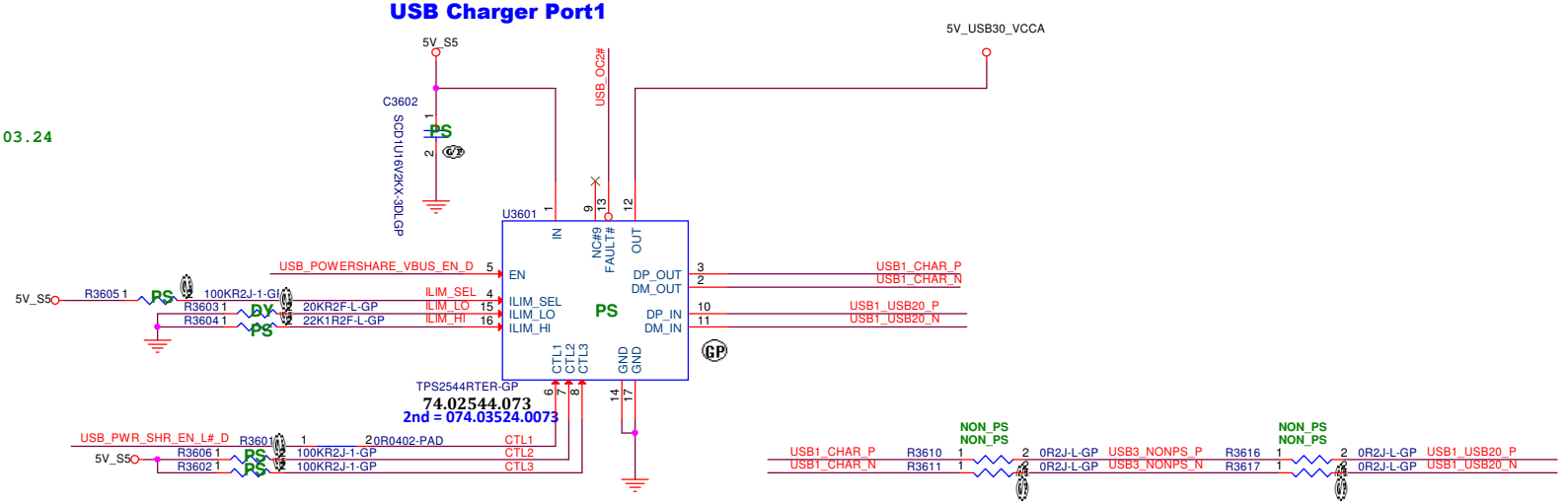
Title: **USB3.0 CONN**

Size: A2 | Document Number: **Mockingbird CML** | Rev: **SC**

Date: Monday, December 09, 2019 | Sheet 35 of 106

Main Func = USB Charger

USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_typ}\,(mA) = \frac{50{,}500}{(R_{ILIM\_XX}\,(k\Omega) + 0.1)}$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

[16] USB1_CHAR_P
[16] USB1_CHAR_N

[35] USB1_USB20_N
[35] USB1_USB20_P

[24] USB_POWERSHARE_VBUS_EN_D
[24] USB_PWR_SHR_EN_L#_D

[16,35] USB_OC2#

<Core Design>

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Title: USB Charger

Size: Custom | Document Number: Mockingbird CML | Rev: SC

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<Core Design>

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Title

USB3.0 PORT

Size	Document Number	Rev
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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	***Mockingbird CML***	***SC***

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<Core Design>

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Title: (RSVD)

Size: A2 | Document Number: Mockingbird CML | Rev: SC

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Main Func = Power Plane & Sequence

5V_S0 & 3D3V_S0

[17,55,81] PM_SLP_S3#

HW_SHUTDOWN

[45] 3V_5V_EN

[26] PURE_HW_SHUTDOWN#

[24] ALWON

POWER GOOD

[51] 1D2V_VTT_PWRGD

VCCIO & VCCSTG

[21] GPPC_H18_BOOTMPC

[17,24,44,46] VCCST_PWRGD

VCCST_CPU

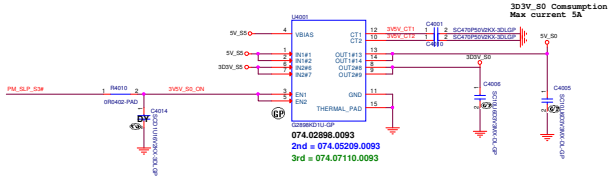
[17,51,65] PM_SLP_S4#

[17,61,62,63,66,76,91] PLT_RST#

ROSA Run Power

5V_S0
5V_S0 Comsumption
Max current 4A

3D3V_S0
3D3V_S0 Comsumption
Max current 5A



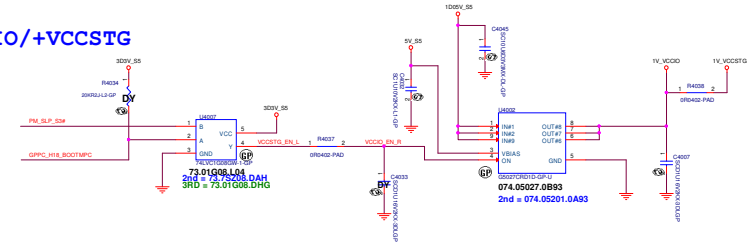
074.02898.0093
2nd = 074.05209.0093
3rd = 074.07110.0093

ROSA Run Power

Power Good

Vinafix.com

+VCCIO/+VCCSTG

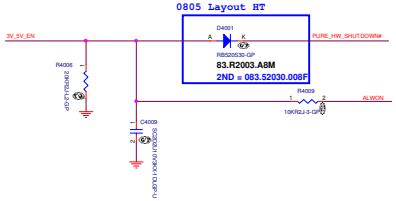


73.01G08.L0A
2nd = 73.25208.DAH
3RD = 73.01G08.DHG

074.05027.0B93
2nd = 074.05201.0A93

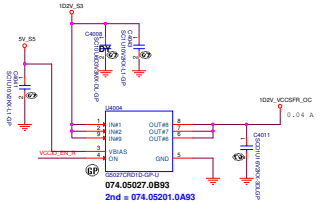
VCCSTG should only ramp up equal to or after VCCST.

0805 Layout HT



83.R2003.A8M
2ND = 083.52030.008F

1D2V_VCCSFR_OC



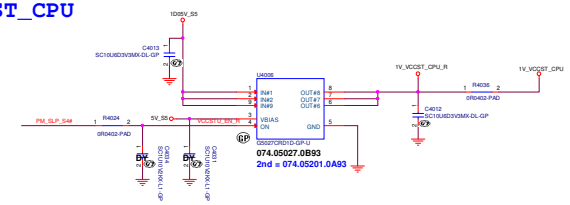
074.05027.0B93
2nd = 074.05201.0A93

MANAGEMENT RAIL POWER GENERATION

VCCST_CPU

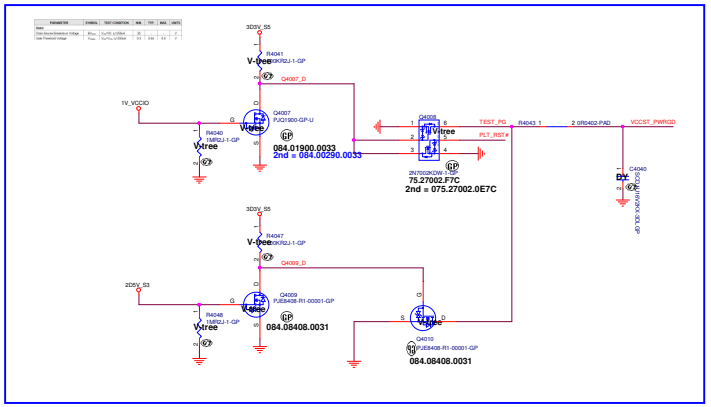
VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST_CPU



074.05027.0B93
2nd = 074.05201.0A93

V-tree_VCCIO



084.01900.0033
2nd = 084.00290.0033

75.27002.F7C
2nd = 075.27002.0E7C

084.08408.0031

084.08408.0031

SA-20190807

<Core Design>

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Title

Connected_Standby(1/2)+DS3

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<Core Design>

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Title: *Connected_Standby(2/2)*

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[24,44] AC_DIS

[17,44] ACOK_IN_M

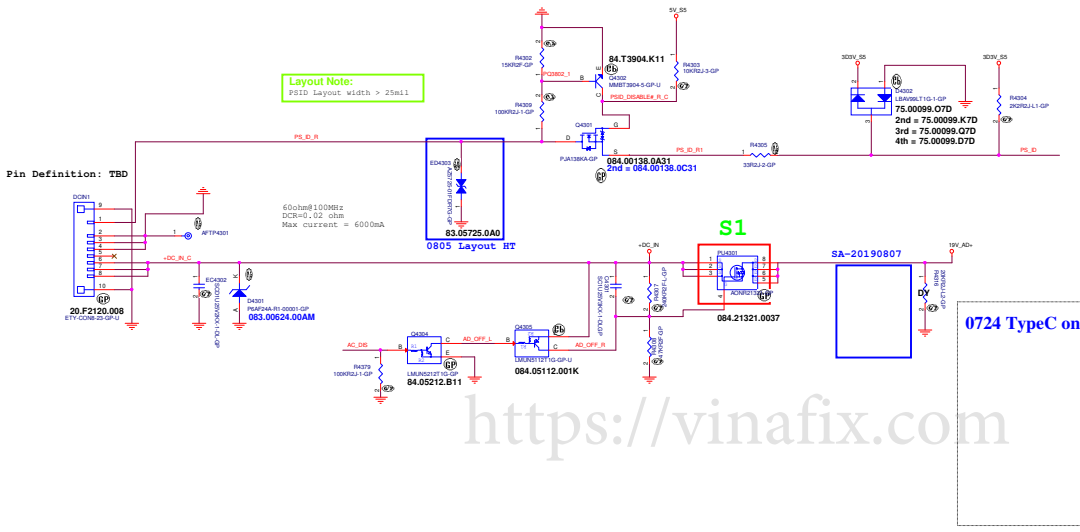
[24] PS_ID

[24,44] HW_ACAVIN_NB

[44,89] +DC_IN_C

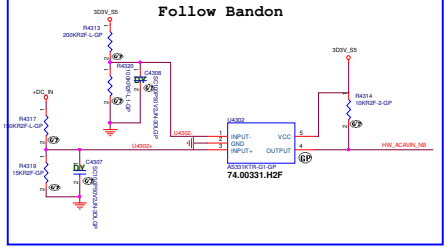
[44,89] +DC_IN

Main Func = ADT Input



0724 TypeC only

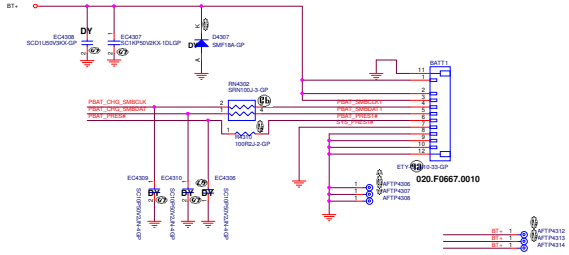
Barrel Adapter Piug-in Detect
Follow Bandon



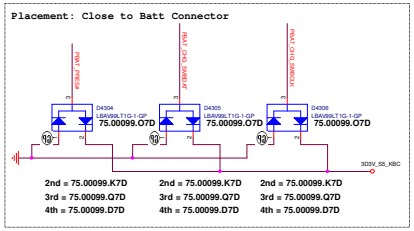
SA-20190807

Main Func = M-BAT Input

Batt Connecter



Placement: Close to Batt Connector



[24,44] PBAT_CHG_SMBCLK

[24,44] PBAT_CHG_SMBDAT

[24,44] PBAT_PRES#

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Title: DCIN		
Size: A1	Document Number: Mockingbird CML	Rev: SC
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ISL9538C For Charger

Main Func = Charger

OFFPAGE

EE needs check it!!

- I2C form EC
- To EC
- From KKP ACK
- E3

ISL9538 AMON/BMON to EC

S2

+3D3V_VDD_DCIN

Vcore_OVP

DCR=8mm-9m Ohm, Idc=13A, Isat=16A 10.0mm x 11.5mm x 3.0mm

0523

PU 3V3_AON_S0 on GPU side

PU +VCCSTG = 1.0 V on CPU side

TypeC Prochot Follow custormer circuits.

CHECK EE follow custormer circuits.

TABLE 22. PROG PIN PROGRAMMING OPTIONS

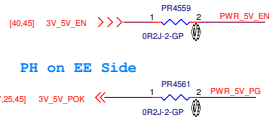
PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

Wistron Corporation
Power (Charger_ISL9538C)
Mockingbird CML

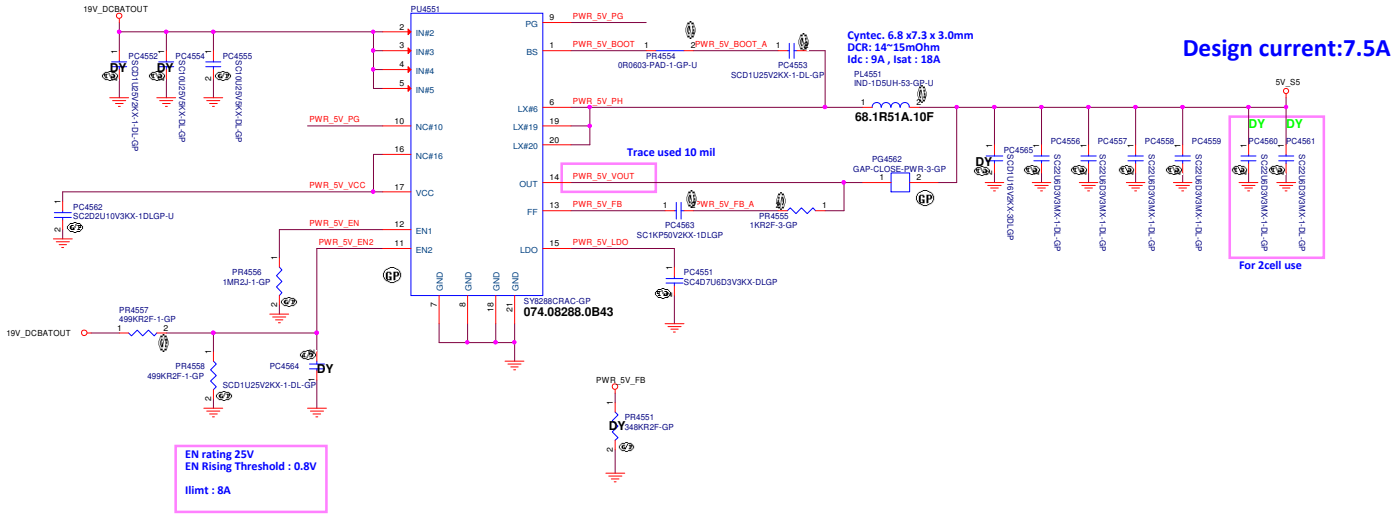
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

OFFPAGE-GAP



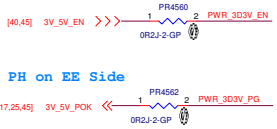
SY8288C For 5V

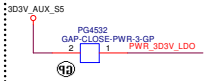


SSID = PWR.Plane.Regulator_3D3V

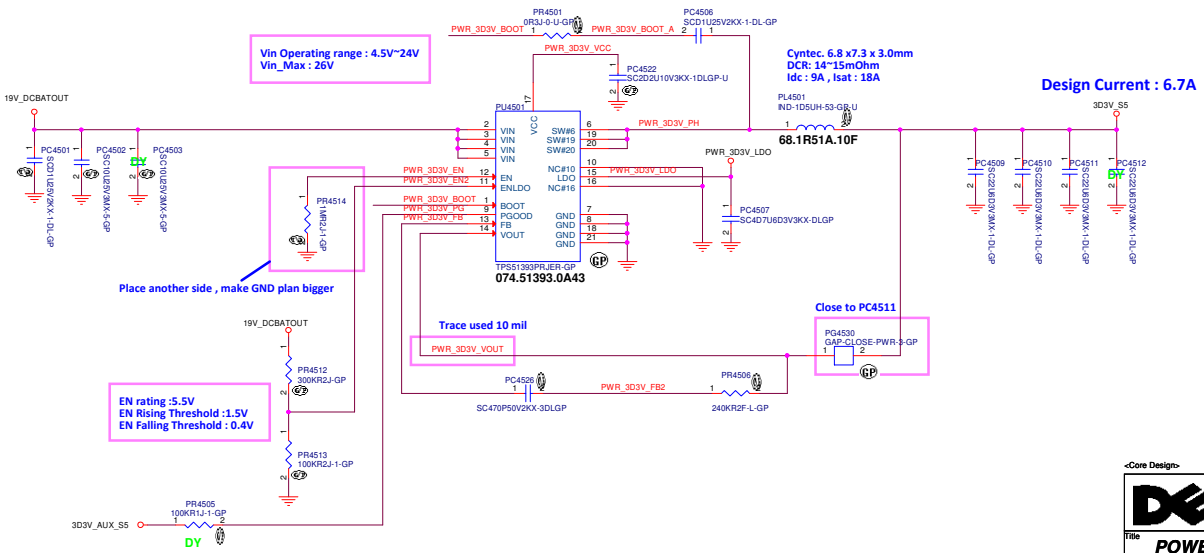
OFFPAGE-Signal

OFFPAGE-GAP





TPS51393 For 3D3V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (8288_5V/51393_3D3V)

Size: A2 | Document Number: Moclingbird CML-U | Rev: SC

Date: Monday, December 09, 2019 | Sheet 45 of 105

Main Func = CPU_CORE

OFFPAGE

PH on CPU side

[3,24,44] PROCHOT#_CPU

[7] SVID_ALERT#_CPU

[7] SVID_CLK_CPU

[7] SVID_DATA_CPU

[17,44] PWR_IMVP_PWRGD

[17,24,40,44] VCCST_PWRGD

For VCCGT Sense

[8] VSSGT_SENSE

[8] VCCGT_SENSE

For Vcore Sense

[7] VCCCORE_SENSE

[7] VSSCORE_SENSE

For Vccsa Sense

[8] VSSSA_SENSE

[8] VCCSA_SENSE

EE side Link
SVID Pull High V

1V_VCCST_CPU — PC4601 GAP-CLOSE_PWR-2-GP — PWR_CORE_VCCST

[47] PWR_VCORE_PWMB

[47] PWR_VCORE_ISUMN

[47] PWR_VCORE_ISUMP

[47] PWR_VCORE_FCCM#

[47] PWR_VCORE_PWMA

[48] PWR_VCCGT_PWM

[48] PWR_VCCGT_FCCM#

[48] PWR_VCCGT_ISUMN

[48] PWR_VCCGT_ISUMP

[50] PWR_VCCSA_ISUMP

[50] PWR_VCCSA_ISUMN

[50] PWR_VCCSA_PWM

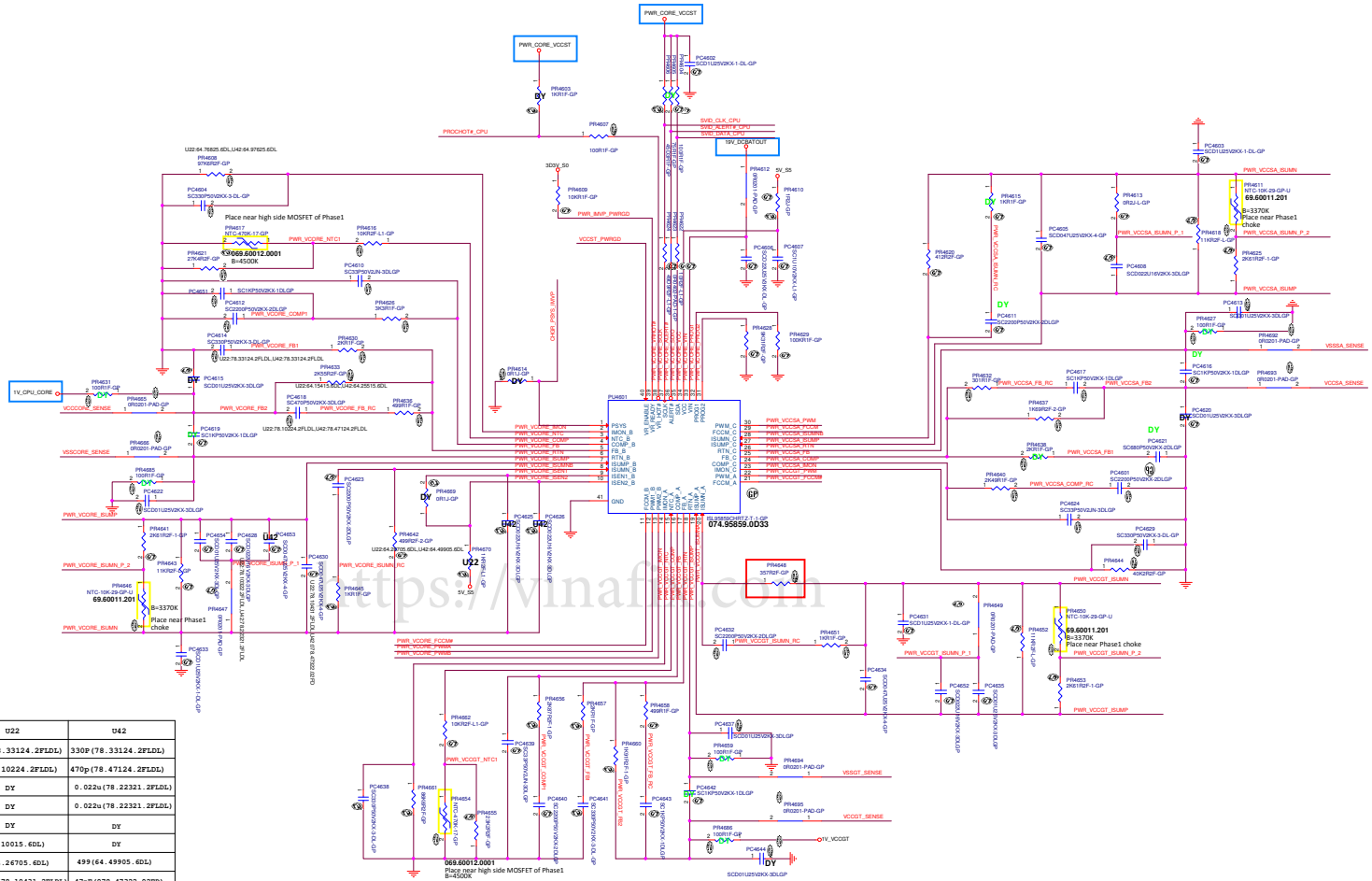
[50] PWR_VCCSA_FCCM

[47] PWR_VCORE_ISEN1

[47] PWR_VCORE_ISEN2

[44] CHGR_PSYS_IMVP

ISL95859C For CPUCORE



	U22	U42
PC4614	330P(78.33124.2FLDL)	330P(78.33124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4670	1K(64.10015.6DL)	DY
PR4642	267(64.26705.6DL)	499(64.49905.6DL)
PC4630	0.1uF(78.10431.2FLDL)	47nF(078.47322.02FD)
PC4628	0.01uF(78.10322.2FLDL)	22nF(78.22321.2FLDL)
PC4654	DY	0.01uF(78.10322.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)
PR4608	76.8K(64.76825.6DL)	97.6K (64.97625.6DL)

<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: POWER (95859_CPUCORE(1/3))

Size: A1 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2013 | Sheet 46 of 106

Main Func = CPU_CORE

AOZ5516Q For VCORE

OFFPAGE

19V_DCBATOUT

PWR_DCBATOUT_VCOREA

PG4721 GAP-CLOSE-PWR-3-GP
PG4722 GAP-CLOSE-PWR-3-GP
PG4723 GAP-CLOSE-PWR-3-GP
PG4724 GAP-CLOSE-PWR-3-GP
PG4725 GAP-CLOSE-PWR-3-GP
PG4726 GAP-CLOSE-PWR-3-GP
PG4727 GAP-CLOSE-PWR-3-GP
PG4728 GAP-CLOSE-PWR-3-GP
R4703 DY D01R6F-3-GP

PWR_DCBATOUT_VCOREA

PC4702 PC4703 PC4705 SC10U25V3MX-5-GP

For acoustic noise

PWR_DCBATOUT_VCOREA

TC4701 ST330U25VDM-5-GP
077.23361.0001

[46] PWR_VCORE_PWMA
[46,47] PWR_VCORE_FCCM#
[46,47] PWR_VCORE_ISEN1
[46,47] PWR_VCORE_ISUMP
[46,47] PWR_VCORE_ISUMN
[46,47] PWR_VCORE_ISEN2

PWR_DCBATOUT_VCOREA

PC4716 PC4717 PC4715 SC10U25V3MX-5-GP

[46] PWR_VCORE_PWMB
[46,47] PWR_VCORE_FCCM#
[46,47] PWR_VCORE_ISEN2
[46,47] PWR_VCORE_ISUMP
[46,47] PWR_VCORE_ISUMN
[46,47] PWR_VCORE_ISEN1

5V_S5

PR4703 2D2R2F-GP
PC4777 SC1U10V2KX-L-GP
PWR_VCORE_VCCDA
PC4709 SC1U10V2KX-L-GP

PR4702 0R0201-PAD-GP
PWR_VCORE_PWMA
PR4717 5K11R1F-GP DY
PR4706 0R0201-PAD-GP
PWR_VCORE_FCCM#

PU4701 AOZ5516QI-GP 074.05516.0073

PWR_VCORE_PWMA_RA
PWR_VCORE_FCCM#_RA
PWR_VCORE_BOOTA
PWR_VCORE_BOOTATRA
PWR_VCORE_SWA
PWR_DCBATOUT_VCOREA

PR4704 2D2R3F-L-GP
PC4708 SCD22U25V3KX-DL-GP
PWR_VCORE_BOOTA_RC

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 37A , Isat : 41A

PL4701 COIL-D15UH-7-GP 068.R1510.2041

PR4705 2D2R6J-3-GP DY
PWR_VCORE_SNB1
PC4710 SC1KP50V2KX-1DLGP DY
PG4708 GAP-CLOSE-PWR-3-GP
PG4709 GAP-CLOSE-PWR-3-GP

1V_CPU_CORE

PT4701 SE330U2VDM-4-GP 79.33719.20C

KBL-R_U42_15W
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)

PWR_VCORE_ISEN1
PR4721 100KR1F-GP
PWR_VCORE_ISUMP
PR4708 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN2
PWR_VCORE_ISUMP_GA
PWR_VCORE_ISUMN_GA
PR4709 10R1F-GP
PR4722 100KR1F-GP DY

5V_S5

PR4713 2D2R2F-GP
PC4766 SC1U10V2KX-L1-GP
PWR_VCORE_VCCDB
PC4712 SC1U10V2KX-L1-GP

PR4711 0R0201-PAD-GP
PWR_VCORE_PWMB
PR4718 5K11R1F-GP DY
PR4712 0R0201-PAD-GP
PWR_VCORE_FCCM#

PU4702 AOZ5516QI-GP 074.05516.0073

PWR_VCORE_PWMB_RA
PWR_VCORE_FCCM#_RB
PWR_VCORE_BOOTB
PWR_VCORE_BOOTBTRB
PWR_VCORE_SWB
PWR_DCBATOUT_VCOREA

PR4710 2D2R3F-L-GP
PC4711 SCD22U25V3KX-DL-GP
PWR_VCORE_BOOTB_RC

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 37A , Isat : 41A

PL4702 COIL-D15UH-7-GP 068.R1510.2041

PR4714 2D2R6J-3-GP DY
PWR_VCORE_SNB2
PC4713 SC1KP50V2KX-1DLGP DY
PG4713 GAP-CLOSE-PWR-3-GP
PG4715 GAP-CLOSE-PWR-3-GP

1V_CPU_CORE

PT4703 SE330U2VDM-4-GP 79.33719.20C

PWR_VCORE_ISEN2
PR4723 100KR1F-GP
PWR_VCORE_ISUMP
PR4716 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP_GB
PWR_VCORE_ISUMN_GB
PR4715 10R1F-GP
PR4724 100KR1F-GP DY

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (5516_CPU_VCORE(2/3))
Size: A2
Document Number: Mockingbird CML
Rev: SC
Date: Monday, December 09, 2019
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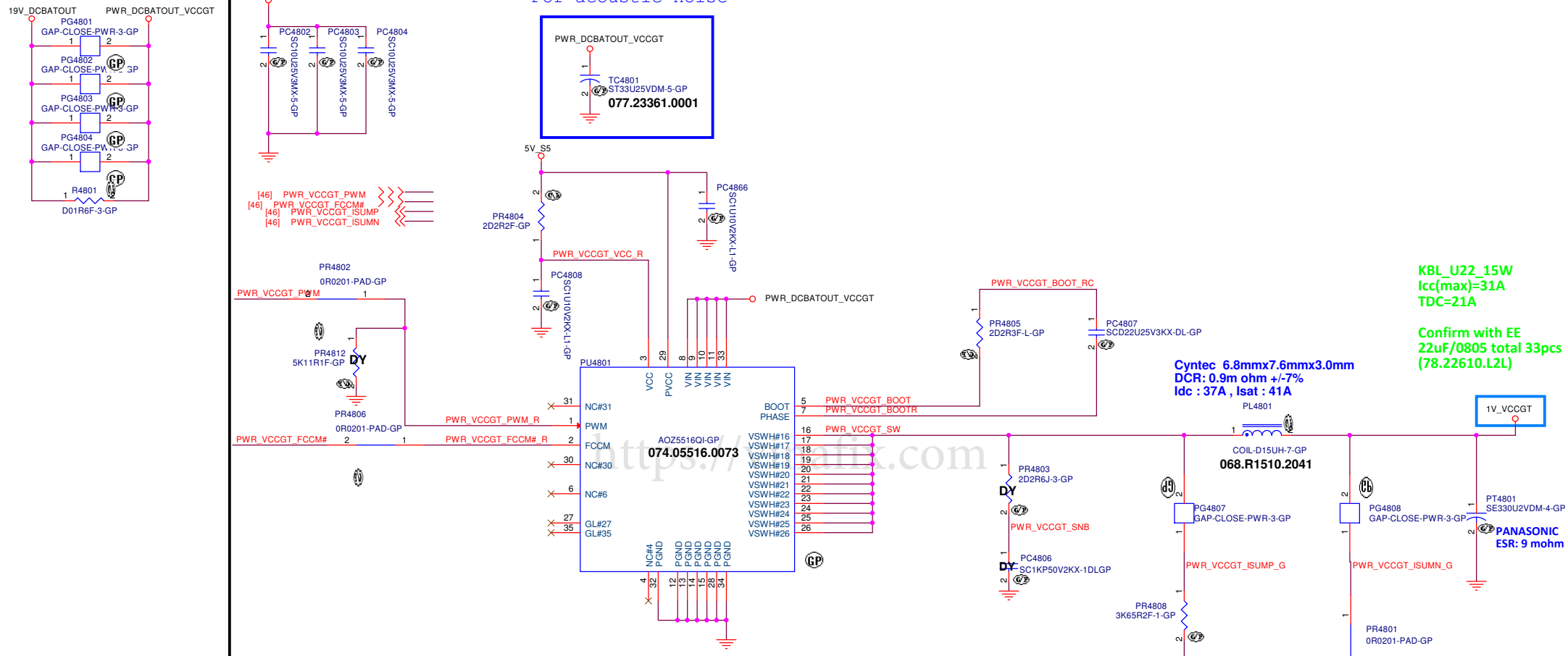
Main Func = CPU_CORE

Offpage-Signal

AOZ5516Q For VCCGT

For acoustic noise



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWER (5516_CPU_VCORE(3/3))		
Size: A3	Document Number: Mockingbird CML	Rev: SC
Date: Monday, December 09, 2019	Sheet 48 of 106	

RSVD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (CPU_VCCGTS_RSVD)

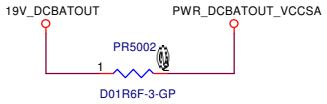
Size: A3 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 49 of 106

Main Func = CPU_CORE

ISL95808 For VCCSA

OFFPAGE



[46] PWR_VCCSA_PWM
[46] PWR_VCCSA_FCCM
[46] PWR_VCCSA_ISUMP
[46] PWR_VCCSA_ISUMN

PWR_DCBATOUT_VCCSA

SKL_U22_15W
Icc(max)=4.5A
TDC=3.7A

Confirm with EE
22uF/0805 total 6pcs
(78.22610.L2L)

PC5002 SC10U25V5KX-DL-GP
PC5003 SC10U25V5KX-DL-GP
EC5004 SCD1U25V2KX-1-DL-GP

PU5001
AONR32320C-GP
084.32320.0037

PWR_VCCSA_BST_RC
PR5001
2D2R3F-L-GP
PC5005
SCD22U25V3KX-DL-GP

PU5002
PWR_VCCSA_DRVH
PWR_VCCSA_BST
PWR_VCCSA_PWM
UGATE
BOOT
PWM
GND
PHASE
FCCM
VCC
LGATE
GND
PWR_VCCSA_SW
PWR_VCCSA_FCCM
5V_S5
ISL95808HRZ-T-1-GP
074.95808.0B73

PC5001
SC2D2U10V3KX-1DLGP-U

PU5003
AONR32320C-GP
084.32320.0037

PWR_VCCSA_DRVL

Cyntec. 7mm x 7mm x 3mm
DCR: 4~4.2 mohm
Idc : 17.5A , Isat : 26A

PL5001
IND-D47UH-22-GP-U
1V_VCCSA

PG5011
GAP-CLOSE-PWR-3-GP
PG5001
GAP-CLOSE-PWR-3-GP

PWR_VCCSA_ISUMP_R
PWR_VCCSA_ISUMN_R

PR5003
3K65R2F-1-GP
PR5004
0R0201-PAD-GP

PWR_VCCSA_ISUMP
PWR_VCCSA_ISUMN

If no need support PS4 mode
please change to ISL6208C
74.06208.B73

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (ISL95808_VCCSA)
Size: A3
Document Number: Mockingbird CML
Rev: SC
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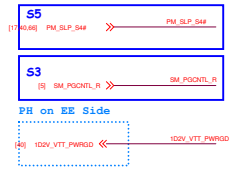
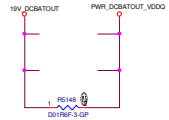
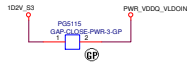
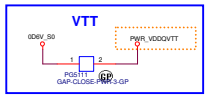
OFFPAGE

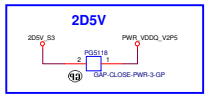


OFFPAGE_GAP









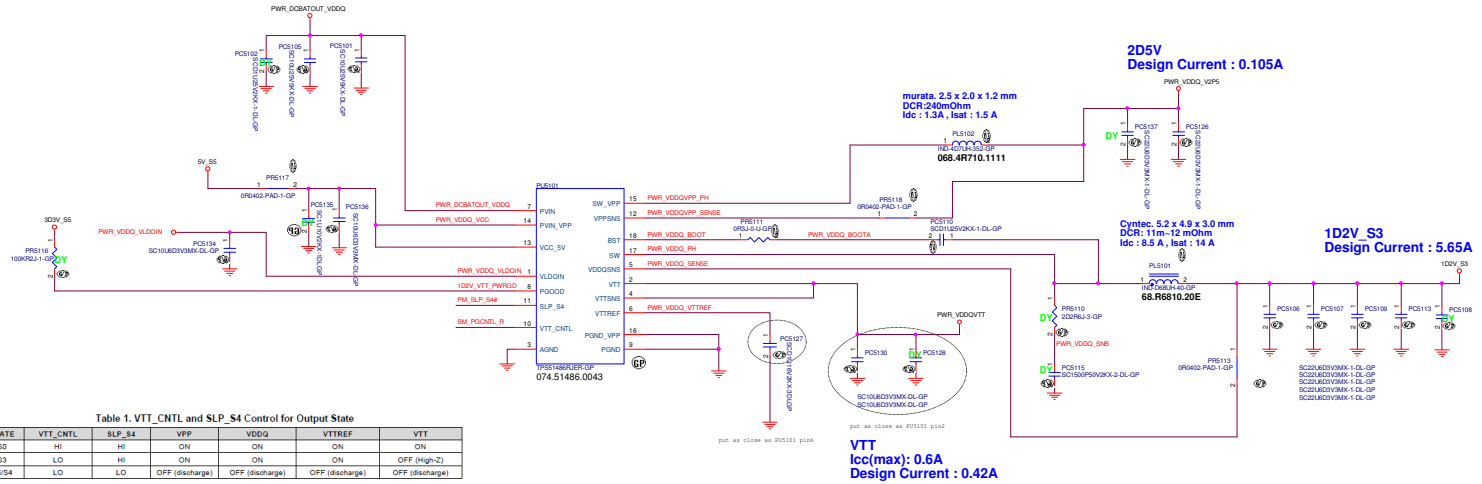


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: 051_POWER (TPS51486R_VDDQ/VTT)
Size: Custom | Document Number: MockingBird CML | Rev: SC
Date: Monday, December 09, 2013 | Sheet 51 of 106

SSID = PWR.Plane.Regulator_1D0V

OFFPAGE-Signal

PH on EE Side

[25,53] 3V_5V_DSW_OK → PR5210 150KR2J-GP → PWR_1D05V_EN

fine tune power sequence

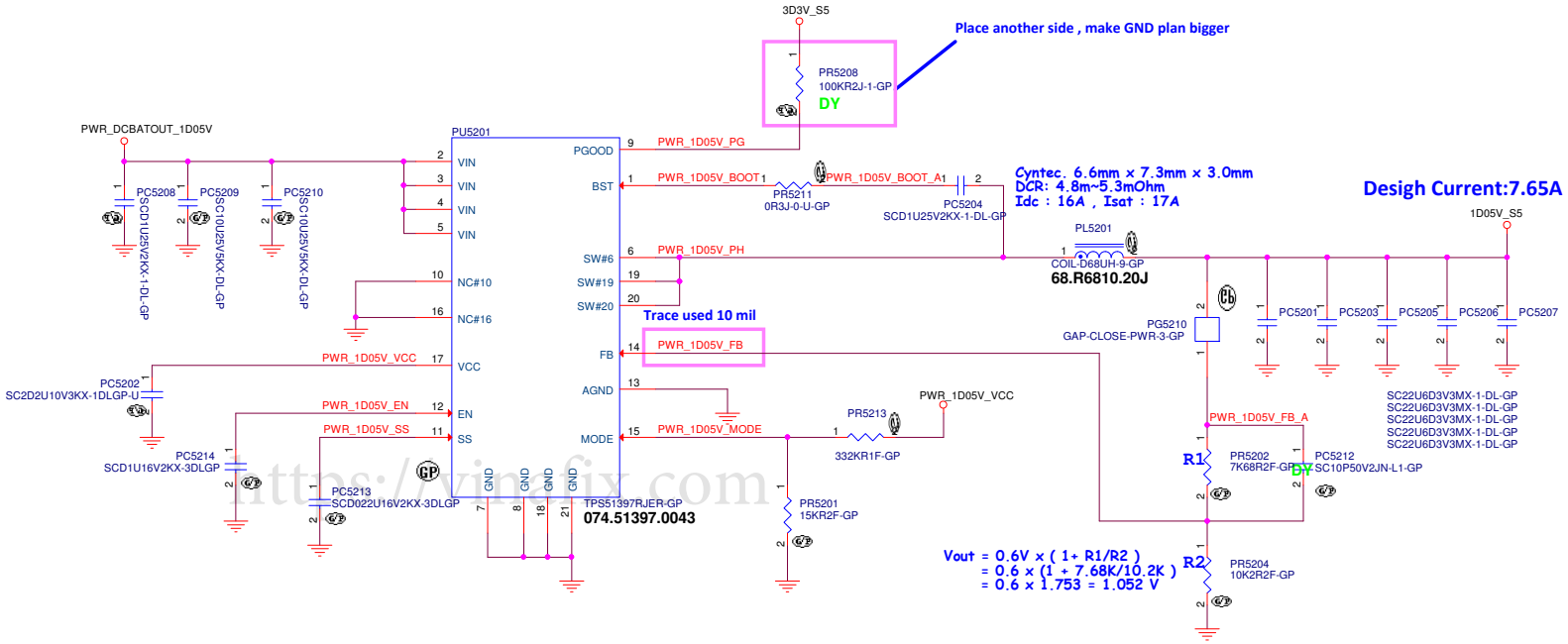
OFFPAGE-GAP

19V_DCBATOUT → PWR_DCBATOUT_1D05V

PG5201 GAP-CLOSE-PWR-3-GP

PG5202 GAP-CLOSE-PWR-3-GP

PG5203 GAP-CLOSE-PWR-3-GP



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (TPS51397_1D05V)

Size: Custom | Document Number: Mockingbird CML-U | Rev: SC

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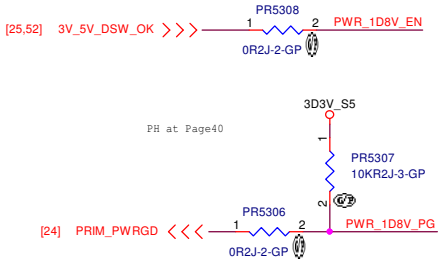
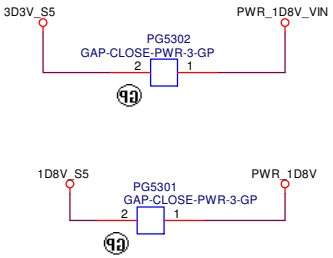
Main Func = 1D8V

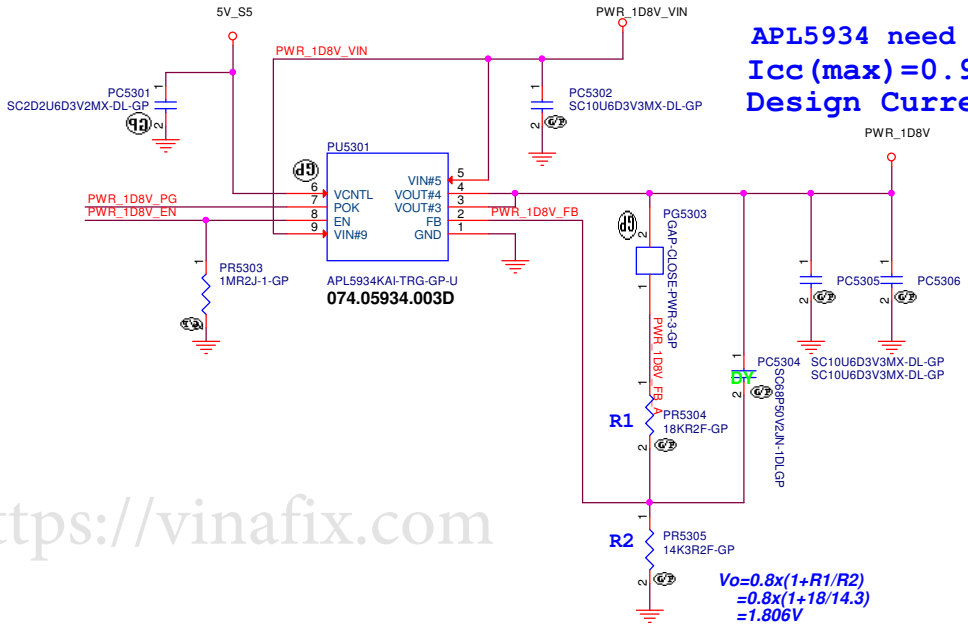
OFFPAGE



OFFPAGE_GAP



APL5934 for 1D8V



APL5934 need <1.8W
Icc(max)=0.95A
Design Current=0.82A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (APL5934_1D8V)

Size: A3 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 53 of

Main Func = 2D5V/ 1D8V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 054_LDO-V1D8V&2D5V

Size: A3 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 54 of 106

Main Func = LCD

From CPU

[4] eDP_TX_CPU_N0
[4] eDP_TX_CPU_P0
[4] eDP_TX_CPU_N1
[4] eDP_TX_CPU_P1
[4] eDP_AUX_CPU_P
[4] eDP_AUX_CPU_N
[4] eDP_HPD_CPU
[4] EDP_VDD_EN
[4] L_BKLT_CTRL

From EC

[24] PANEL_BKEN
[20,21] LCD_CBL_DET#
[17,40,81] PM_SLP_S3#
[19] TOUCH_DETECT#

FOR TESTING

[20] DBC_PANEL_EN
[24] LCD_VCC_TEST_EN
[24] LCD_TST
[24] CABLE2_OCP#
[24] PANEL_MONITOR
[66] 3D3V_LCDVDD_R
[20,70] SENSOR_I2C_SDA
[20,70] SENSOR_I2C_SCL
[20] GSEN_INT1_C

0513

Main Func = Touch panel

[20] CPU_I2C_SDA_TS
[20] CPU_I2C_SCL_TS
[21] TOUCH_PANEL_PD#
[3] TOUCH_PANEL_INTR#
[24] TOUCH_REPORT_SW

Main Func = CAMERA

[4] IR_CAM_DET#
[16] CCD_USB20_N
[16] CCD_USB20_P
[27] DMIC_SCL_CODEC
[27] DMIC_SDA_CODEC
[19] DMIC_PCH_CLK
[19] DMIC_PCH_DATA

INVERTER POWER

19V_DCBATOUT
DCBATOUT_LCD_R
R5566 D01R6F-3-GP
F5503 PCMSW-1D1A24V-GP-U
69.50007.A31
2nd = 69.50007.D31
C5512 C5513
DCBATOUT_LCD
2019.08.06
Starload height limite change to 0603 package
2015/09/24 modify

3D3V_S0
R5517 4K7R2J-3-GP TS_I2C
R5518 4K7R2J-2-GP TS_I2C
CPU_I2C_SCL_TS
CPU_I2C_SDA_TS

LCD_CBL_DET#
0=LCD cable connect
1=LCD cable not connect

IR_CAM_DET#
0=IR Camera connect
1=IR Camera not connect

TOUCH_I2C_DET#
0=I2C
1=OSB

Hinge up cable protection

EDP_VDD_EN
D5502 RB520S30-GP
LCDVDD_EN
83.R2003.A8M
2ND = 083.52030.008F
LCD_VCC_TEST_EN
D5506 RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
0614 Layout HT

3D3V_S5
5V_S5
LCDVDD_EN
PM_SLP_S3#
U5501 SI2895ALX21U-GP
3D3V_LCDVDD_R
CABLE1_OCP#
CABLE2_R_OCP#
3D3V_HINGE_N

SA-20190806
CABLE1_OCP# R527 1 2 0R0402-PAD CABLE2_OCP#
CABLE2_R_OCP# R528 1 2 0R0402-PAD

3D3V_HINGE_S0
3D3V_HINGE_R R5564 D01R6F-3-GP

Near LCD1 connector

SA-20190729

3D3V_LCDVDD_S0
3D3V_LCDVDD_R R5563 D01R6F-3-GP

5V_TPAN_VDD
PM_SLP_S3# R5571 100KR2J-1-GP
TP_PWR_EN
SV_PEN_R
U5502 GS77AHTPTU1GP
Current Limit Type 0.19A
074.51711.009P
CABLE2_OCP# R572 0R0402-PAD
5V_S5
R5574 100R2J-2-GP
RSET R5573 110KR2F-GP

Brightness

EC (BIST MODE)

L_BKLT_CTRL
LCD_TST
eDP_HPD_CPU
D5503 BAT54C-12-GP
75.00054.A7D
PANEL_BKEN
BKLT_CTRL
LCD_TST
RN5503 SRN100KJ-4-GP
PLON_OUT_C
LCD_BRIGHTNESS
LCD_TST_C
EDP_HPD_CONN
LCDVDD_EN
RN5502 SRN100KJ-5-GP

Touch Panel / CCD& CAM / Sensor Board / Display / eDP

DCBATOUT_LCD
Touch Panel 5V_TPAN_VDD
Sensor 3D3V_HINGE_S0
DMIC 3D3V_HINGE_S0
TOUCH_PANEL_INTR#
R5544 100KR2J-1-GP
5V_IRLED
DMIC_CLK_EDP
DMIC_DATA_EDP
CCD_USB20_CON_N
CCD_USB20_CON_P
IR_CAM_DET#
SENSOR_I2C_SCL
SENSOR_I2C_SDA
GSEN_INT1_C
3D3V_LCDVDD_S0
Trace width = 80mil
DBC_PANEL_EN R5504 2 100R2J-2-GP
LCD_EN_H
EDP_HPD_CONN
LCD_TST_C
LCD_BRIGHTNESS
BLON_OUT_C
LCD_CBL_DET#
eDP_TX_CPU_P0 C5524 SCD1U16V2KX-3DLGP eDP_TX_CON_P0
eDP_TX_CPU_N0 C5525 SCD1U16V2KX-3DLGP eDP_TX_CON_N0
eDP_TX_CPU_P1 C5522 SCD1U16V2KX-3DLGP eDP_TX_CON_P1
eDP_TX_CPU_N1 C5523 SCD1U16V2KX-3DLGP eDP_TX_CON_N1
eDP_AUX_CPU_P C5526 SCD1U16V2KX-3DLGP eDP_AUX_CON_P
eDP_AUX_CPU_N C5521 SCD1U16V2KX-3DLGP eDP_AUX_CON_N
LCD1 STAR-CON40-S-GP
020.F0847.0040
2nd = 20.F2406.040

PANEL_PWRGD CIRCUIT

2018.10.21
19V_DCBATOUT R5551 0R0402-PAD Q5502_E
Q5502 MMBT3906-3-GP
84.03906.R11
2nd = 84.T3906.E11
R5554 10KR2F-2-GP
R5546 4K7R2F-GP
D5504 RB520S30-GP
DCBATOUT_LCD_PWRGD
83.R2003.A8M
2ND = 083.52030.008F
R5555 200KR2F-L-GP
C5531 SC2200P50V2KX-2DLGP
DCBATOUT_LCD_PG
Q5505 LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.03904.K11
3D3V_S5
R5547 100KR2F-L1-GP
PANEL_PWRGD_R
R5549 1MR2F-GP
2018.10.21
R5545 0R0402-PAD
PANEL_MONITOR
C5529 SCD1U16V2KX-3DLGP

3D3V_S0 R5550 0R0402-PAD 2018.10.21 Q5501_E
Q5501 MMBT3906-3-GP
84.03906.R11
2nd = 84.T3906.E11
Q5501_B
R5553 10KR2F-2-GP
R5561 4K7R2F-GP
D5505 RB520S30-GP
LCDVDD_PWRGD
83.R2003.A8M
2ND = 083.52030.008F
R5552 200KR2F-L-GP
C5535 SC2200P50V2KX-2DLGP
LCDVDD_PG
Q5504 LMBT3904LT1G-GP
84.T3904.H11
2nd = 84.03904.K11

Gen 10 LCD-BIST
Check if 3V and B+ is power on before doing panel self-test. It's using for judge MB or panel damaged.

2018.04.17 add

IR LED POWER

5V_S0
2018.10.05
F5506 MKB_L
5V_IRLED
C5504 SC4D7U6D3V3KX-DLGP
MKB_L

CCD_USB20_N
CCD_USB20_P
EL5501 CLM3R2012PY2D-GP
068.09002.2001
CCD_USB20_CON_N
CCD_USB20_CON_P
ED5502 A2C2099-04S-2-GP
075.09904.0A7C
DY

0514 double check
DMIC_CLK_EDP
DMIC_DATA_EDP
RN5505 SRN33J-5-GP-U
DMIC_PCH_CLK
DMIC_PCH_DATA
RN5504 SRN33J-5-GP-U
DMIC_SCL_CODEC
DMIC_SDA_CODEC
C5553 C5554 SCD1U16V2KX-3DLGP

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: LCD&CAM&DMC&Touch
Size: Custom
Document Number: Mockingbird CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 55 of 108

Main Func = CRT

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT(Reserved)

Size: A3 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 56 of 106

SSID = HDMI Level Shifter/Connector

[4] HDMI_DDI_TX_N0
[4] HDMI_DDI_TX_P0
[4] HDMI_DDI_TX_N1
[4] HDMI_DDI_TX_P1
[4] HDMI_DDI_TX_N2
[4] HDMI_DDI_TX_P2
[4] HDMI_DDI_TX_N3
[4] HDMI_DDI_TX_P3

[4] HDMI_SCL_CPU
[4] HDMI_SDA_CPU
[4] HDMI_HPD_CPU

HDMI_DDI_TX_N3 C5701 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_P3 C5704 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_N0 C5705 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_P0 C5703 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_N1 C5707 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_P1 C5706 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_N2 C5708 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_P2 C5709 SCD1U16V2KX-3DLGP HDMI_DDI_TX_CON_P2

SA-20190724

5V_S0
R5705 470R1F-GP
R5759 470R1F-GP
R5773 470R1F-GP
R5774 470R1F-GP
R5775 470R1F-GP
R5776 470R1F-GP
R5777 470R1F-GP
R5778 470R1F-GP
Q5701 PJE8408-HF-00001-GP
HDMI_PLL_GND

5V_S0
D5701 RB520S30-GP
D5702 RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
83.R2003.A8M
2ND = 083.52030.008F

0614 Layout HT

HDMI_SCL_R
HDMI_SDA_R
RN5702 SRN2K2J-1-GP

3D3V_S0
Part Reference = Q5702
HDMI_SCL_CPU
HDMI_SCL_CON
HDMI_SDA_CPU
HDMI_SDA_CON
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

HDMI_DDI_TX_CON_N0
ER5701 180R2J-1-GP
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N1
ER5702 180R2J-1-GP
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2
ER5703 180R2J-1-GP
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N3
ER5704 180R2J-1-GP
HDMI_DDI_TX_CON_P3

5V_S0
F5701 POLYSW-1D1A6V-9-GP-U
69.48001.081
5V_HDMI
2ND = 69.50011.081
3RD = 69.50013.101

Vinafix.com

HDMI CONN

HDMI1
5V_HDMI
C5702 SCD1U16V2KX-3DLGP
+5V_POWER
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N2
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
HDMI_SCL_CON
HDMI_SDA_CON
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
GND
SKT-HDMI23-211-GP
022.10025.0421

3D3V_S0
HDMI_HPD_B R5710 150KR2F-L-GP HDMI_DET_CON
HDMI_HPD_CPU R5712 0R0402-PAD HDMI_HPD_E
Q5703 LMBT3904LT1G-GP
84.T3904.H11
R5709 100KR2J-1-GP
R5711 200KR2F-L-GP

EMI Request :

ED5701
HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N1
DY
PUSB3F96-GP
2nd = 075.08809.0073
075.PUSB3.0073

ED5702
HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3
HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0
DY
PUSB3F96-GP
2nd = 075.08809.0073
075.PUSB3.0073

ED5703
HDMI_DET_CON
HDMI_SCL_CON
HDMI_SDA_CON
DY
PUSB3F96-GP
2nd = 075.08809.0073
075.PUSB3.0073

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI
Size: Custom
Document Number: Mockingbird CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 57 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A3	*Mockingbird CML*	*SC*

Date: Monday, December 09, 2019 Sheet 58 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: A3 | Document Number: Mockingbird CML | Rev: SC

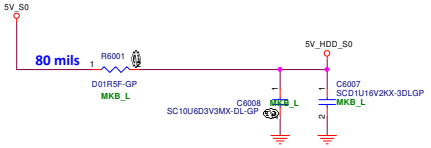
Date: Monday, December 09, 2019 | Sheet 59 of 106

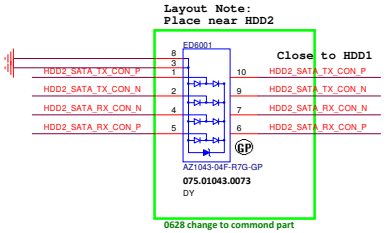
Main Func = HDD

HDD

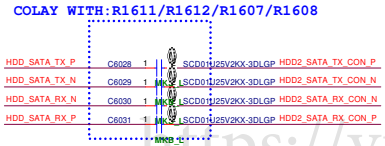
[70] FFS_INT2_Q
[16,60] HDD_DEVSLP
[16] HDD_SATA_TX_P
[16] HDD_SATA_TX_N
[16] HDD_SATA_RX_P
[16] HDD_SATA_RX_N
[16,60] HDD_DEVSLP
[18] HDD_DET#

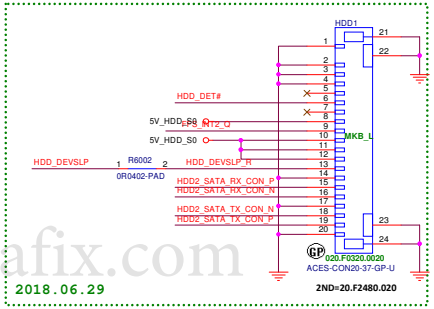
HDD POWER





SATA HDD Connector





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF HDD/ODD

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 60 of 106

Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P
[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P

PCIE_CLK

[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P
[18] WLAN_CLKREQ_CPU_N

USB2.0

[16] BT_USB20_P
[16] BT_USB20_N

Single end

[3] BLUETOOTH_EN
[21] WIFI_RF_EN
[17,40,62,63,66,76,91] PLT_RST#
[18,24] SUS_CLK

Debug

[24,68] HOST_DEBUG_TX

Power EN (Madesimo)

[19] BT_PCMOUT_CLKREQ0
[19] BT_PCMFRM_CRF_RST_N

[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_CLK_DN
[21] CNV_WT_CLK_DP

[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_CLK_DN
[21] CNV_WR_CLK_DP

[15,20] CNV_RGI_DT_R
[20] CNV_BRI_DT_R

[20] CNV_BRI_RSP
[20] CNV_RGI_RSP

[18] JIO3_PCIE_WAKE#
[18] CLKIN_XTAL_LCP_R

SA-20190807

3D3V_WLAN
R6141 10KR2J-3-GP DY
WIFI_RF_EN — R6114 DY 1 — WIFI_RF_EN_R
0R2J-2-GP

3D3V_WLAN
R6142 10KR2J-3-GP DY
BLUETOOTH_EN — R6113 DY 1 — BLUETOOTH_EN_R
0R2J-2-GP

3D3V_S5 — R6140 D01R5F-GP — 3D3V_WLAN

1.1A

C6110 SCD1U16V2KX-3DLGP
C6106 SC10U6D3V3MX-DL-GP
C6109 SCD1U16V2KX-3DLGP

AFTE14P-GP AFTP6101 — 1 3D3V_WLAN
AFTE14P-GP AFTP6105 — 1 WLAN_CLKREQ_CPU_N
AFTE14P-GP AFTP6106 — 1 WIFI_RF_EN_R
AFTE14P-GP AFTP6107 — 1 BLUETOOTH_EN_R
AFTE14P-GP AFTP6108 — 1 PLT_RST#
AFTE14P-GP AFTP6109 — 1 BT_USB20_CON_N
AFTE14P-GP AFTP6110 — 1 BT_USB20_CON_P
AFTE14P-GP AFTP6608 — 1 JIO3_PCIE_WAKE#

3D3V_WLAN

R6106 10KR2J-3-GP — CLKIN_XTAL_LCP_R
WIFI_RF_EN_R
BLUETOOTH_EN_R
PLT_RST#
SUS_CLK — R6135 33R2J-2-GP — SUSCLK_WLAN

CNV_RGI_RSP — R6109 22R2J-2-GP — CNV_RGI_RSP_R
CNV_BRI_RSP — R6118 22R2J-2-GP — CNV_BRI_RSP_R
CNV_BRI_DT_R
CNV_RGI_DT_R

BT_PCMOUT_CLKREQ0
BT_PCMFRM_CRF_RST_N
3D3V_WLAN
R6134 75KR2F-GP
R6133 71K5R2F-1-GP

WLAN1

76	76	77	77
74	3_3VAUX	75	GND
72	3_3VAUX	73	RESERVED#73
70	RESERVED#70	71	RESERVED#71
68	RESERVED#68	69	GND
66	RESERVED#66	67	RESERVED#67/2ND_LANE_PERN1
64	GPIO0_NFC_RESET#/MGPIO7	65	RESERVED#65/2ND_LANE_PERP1
62	NFC_I2C_IRQ/MGPIO5	63	GND
60	NFC_I2C_SM_CLK	61	RESERVED#61/2ND_LANE_PETN1
58	NFC_I2C_SM_DATA	59	RESERVED#59/2ND_LANE_PETP1
56	W_DISABLE#1	57	GND
54	RESERVED#54/W_DISABLE#2	55	PEWAKE0#
52	PERST0#	53	CLKREQ0#
50	SUSCLK_32KHZ	51	GND
48	COEX1	49	REFCLKN0
46	COEX2	47	REFCLKP0
44	COEX3	45	GND
42	CLINK_CLK	43	PERN0
40	CLINK_DATA	41	PERP0
38	CLINK_RESET	39	GND
36	UART_CTS	37	PETN0
34	UART_RTS	35	PETP0
32	UART_TX	33	GND
22	UART_RX	23	SDIO_RESET
20	UART_WAKE	21	SDIO_WAKE
18	GND	19	SDIO_DAT3
16	LED#2	17	SDIO_DAT2
14	PCM_OUT	15	SDIO_DAT1
12	PCM_IN	13	SDIO_DAT0
10	PCM_SYNC	11	SDIO_CMD
8	PCM_CLK	9	SDIO_CLK
6	LED#1	7	GND
4	3_3VAUX	5	USB_D-
2	3_3VAUX	3	USB_D+
		1	GND
NP2	NP2	NP1	NP1

NGFF_KEY_E_75P
SKT-NGFF75P-164-GP
062.10003.0B11

CNV_WT_CLK_DP
CNV_WT_CLK_DN
CNV_WT_DP0
CNV_WT_DN0
CNV_WT_DP1
CNV_WT_DN1
JIO3_PCIE_WAKE#
WLAN_CLKREQ_CPU_N
WLAN_CLK_CPU_N
WLAN_CLK_CPU_P
WLAN_PCIE_RX_N
WLAN_PCIE_RX_P
WLAN_PCIE_TX_CON_N — C6107 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_N
WLAN_PCIE_TX_CON_P — C6108 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_P
CNV_WR_CLK_DP
CNV_WR_CLK_DN
CNV_WR_DP0
CNV_WR_DN0
CNV_WR_DP1
CNV_WR_DN1
BT_USB20_CON_N
BT_USB20_CON_P

BT_USB20_CON_P — R6111 1 2 0R0402-PAD — BT_USB20_P
BT_USB20_CON_N — R6110 1 2 0R0402-PAD — BT_USB20_N

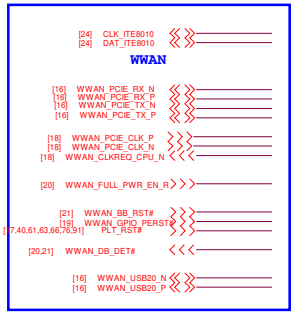
1D8V_S5 — R6115 DY 20KR2J-L2-GP — CNV_BRI_DT_R

<Core Design>

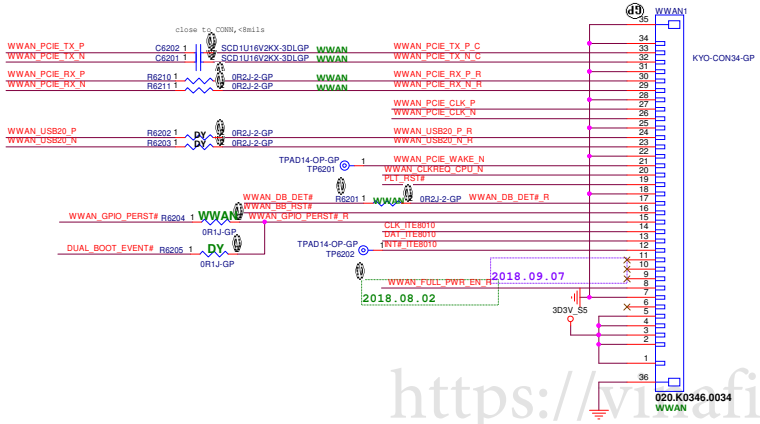
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN CONN
Size: A3
Document Number: Mockingbird CML
Rev: SC
Date: Monday, December 09, 2019
Sheet 61 of 106

Main Func = WWAN



[16] DUAL_BOOT_EVENT#



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA

Size	Document Number	Rev
A2	Mockingbird CML	SC

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Main Func = M.2 SSD

M.2 SSD2

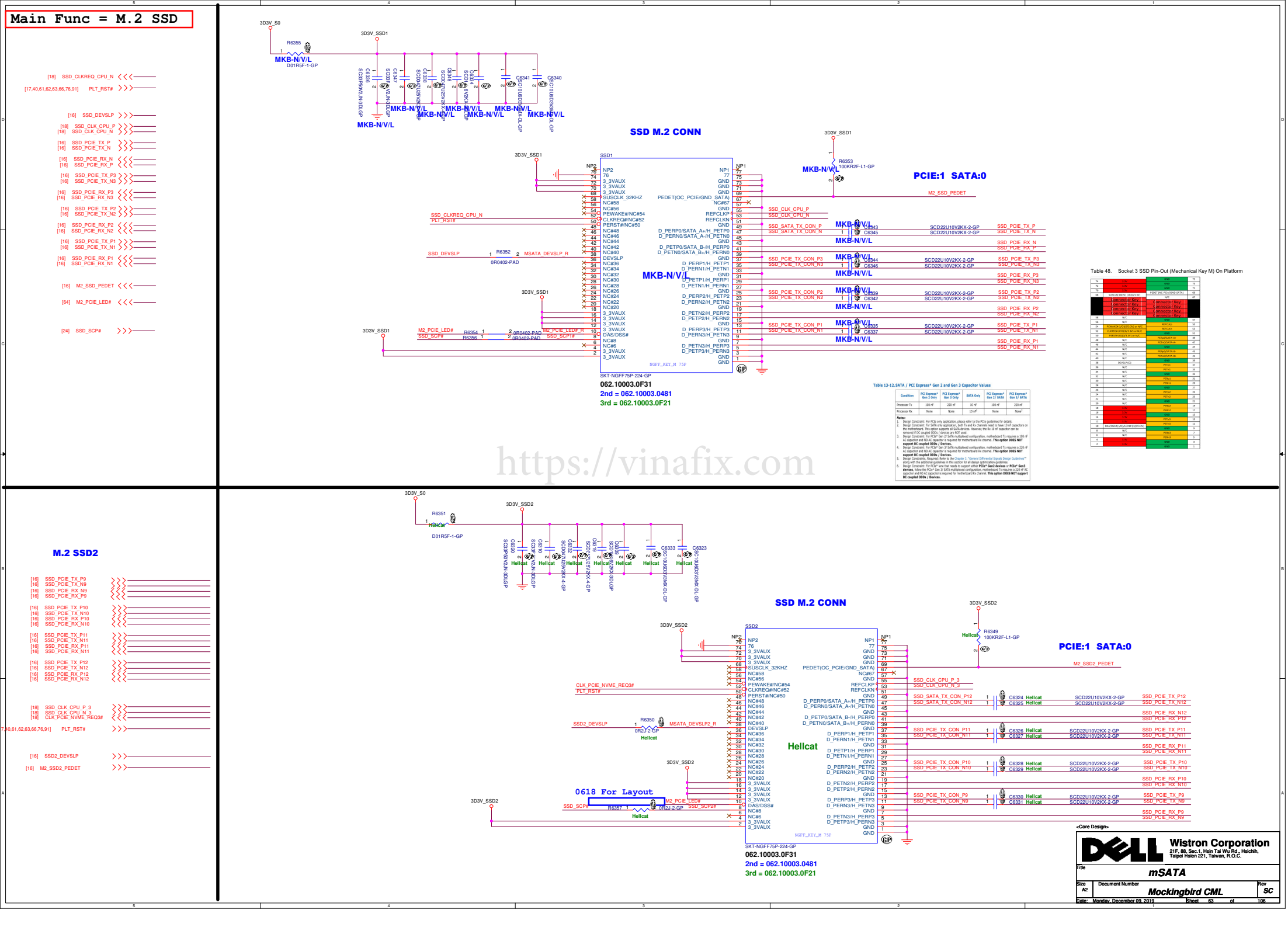


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-12.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA

Size: A2 | Document Number: Mockingbird CML | Rev: SC

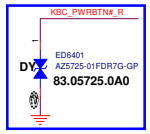
Date: Monday, December 09, 2019 | Sheet 63 of 106

Main Func = Power BTN

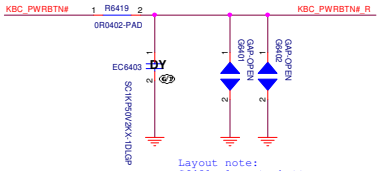
[20,24,66] LID_CL_SIO#
[24] KBC_PWRBTN#
[66] KBC_PWRBTN#_R

NONE FINGER PRINT 才會上件

Power button



0614 Layout HT



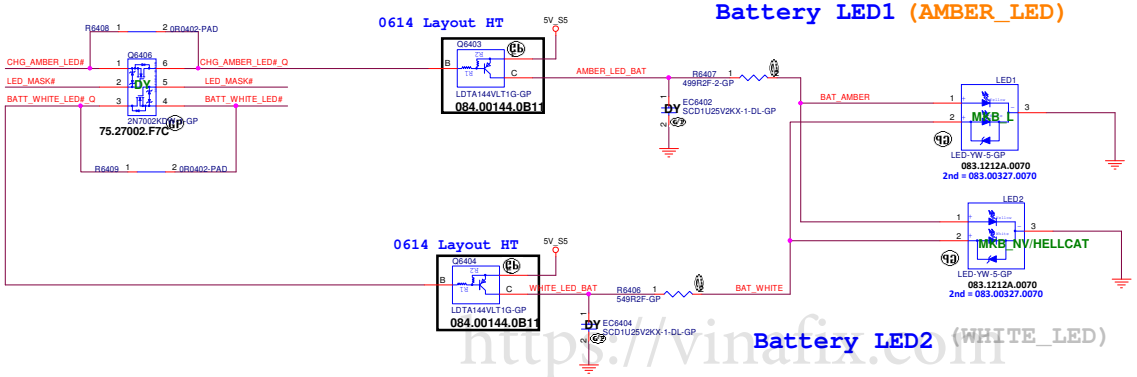
Layout note:
G6401 place to buttom
G6402 place to top

Main Func = Battery LED

Low actived from KBC GPIO

[24,66] LED_MASK#
[24] CHG_AMBER_LED#
[24] BATT_WHITE_LED#

Battery LED1 (AMBER_LED)

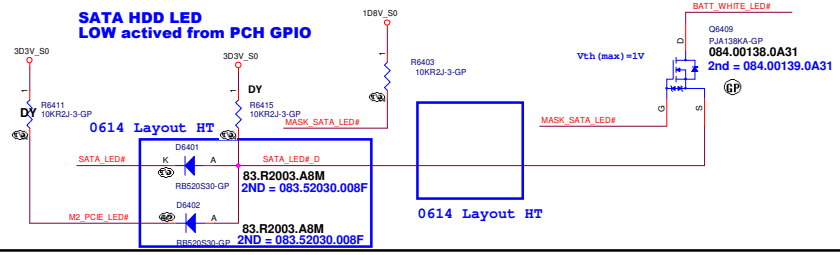


Battery LED2 (WHITE_LED)

Main Func = HDD LED

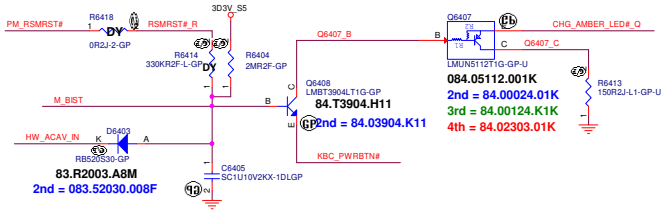
[24] MASK_SATA_LED#
[16] SATA_LED#
[63] M2_PCIE_LED#

SATA HDD LED
LOW actived from PCH GPIO



Main Func = M-BIST

[17] PM_RSMRST#
[24] M_BIST
[24,44] HW_ACAV_IN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button

Size	Document Number	Rev
Custom	Mockingbird CML	SC

Date: Monday, December 09, 2019 Sheet 64 of 106

Main Func = KB

0513

[24] CAP_LED#_R

[20] KB_DET#

[19] KB_LED_BL_DET

[24] KB_LED_PWM

[24] KSO00 KSO00
[24] KSO01 KSO01
[24] KSO02 KSO02
[24] KSO03 KSO03
[24] KSO04 KSO04
[24] KSO05 KSO05
[24] KSO06 KSO06
[24] KSO07 KSO07
[24] KSO08 KSO08
[24] KSO09 KSO09
[24] KSO10 KSO10
[24] KSO11 KSO11
[24] KSO12 KSO12
[24] KSO13 KSO13
[24] KSO14 KSO14
[24] KSO15 KSO15
[24] KSO16 KSO16

[24] KSI[0..7]

KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7

Keyboard Backlight (Reserved)

5V_S0 → F6502 KBBL POLYSW-1D1A6V-9-GP-U 69.48001.081 → +5V_KB_BL

C6501 KBBL SCD1U16V2KX-3DLGP

KB_LED_BL_DET → R6503 KBBL 51KR2J-1-GP

KB_LED_DET_C → KBBL1 KBBL

KB_BL_CTRL# → ACES-CON4-90-GP-U 020.K0298.0004 → AFTP6565

R6507 KBBL 100KR2J-1-GP

KB Backlight Power Consumption: 285mA max.

KB_LED_PWM → R6505 DY 100KR2J-1-GP

Q6501 PJA3402-R1-00001-GP 084.03402.0031 KBBL

+5V_KB_BL → AFTP6605

KB_LED_DET_C → AFTP6606

KB_BL_CTRL# → AFTP6607

KB_LED_DET_C → EC6501 DY SCD1U16V2KX-3DLGP

KB_BL_CTRL# → EC6503 DY SCD1U16V2KX-3DLGP

CAP LED Control

LOW actived from KBC GPIO

CAP_LED#_R → Q6502 LDTA144VLT1G-GP 084.00144.0B11 (5V_S0) → CAP_LED_Q → R6506 1KR2J-1-GP → CAP_LED

Internal Keyboard Connector

KB1

CAP_LED
KSO10
KSO11
KSO09
KSO14
KSO13
KSO15
KSO16
KSO12
KSO00
KSO02
KSO01
KSO03
KSO04
KSO05
KSI0
KSI3
KSI1
KSI2
KSI5
KSI4
KSI6
KSI7
KB_DET#

ACES-CON30-29-GP 020.K0254.0030

Main Func = TPAD

0513

[24] CLK_TP_SIO_I2C_DAT
[24] DAT_TP_SIO_I2C_CLK

[20,66] CPU_I2C_SCL_P0
[20,66] CPU_I2C_SDA_P0

[3,24] TOUCHPAD_INTR#
[24] PTP_DIS#

3D3V_S0 → R6502 0R0402-PAD → TP_VDD

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Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

TP_VDD → TP side has pull high → R6511 10KR2J-3-GP → TOUCHPAD_INTR#

TP_WKAE

Support PTP

PS2

I2C

DAT_TP_SIO_I2C_CLK
CLK_TP_SIO_I2C_DAT
RN6502 SRN0J-6-GP

CPU_I2C_SCL_P0 → R6513 0R0402-PAD → I2C1_SCL_R
CPU_I2C_SDA_P0 → R6512 0R0402-PAD → I2C1_SDA_R

SC12P50V2AN-3GP EC6501 DY
SC12P50V2AN-3GP EC6502 DY

TP_VDD → RN6503 SRN2K2J-1-GP → I2C1_SCL_R, I2C1_SDA_R

Precision Touch Pad Connector

TP_VDD → C6505 SCD1U16V2KX-3DLGP

TP1 PTWO-CON8-16-GP 020.K0255.0008
2nd = 020.K0151.0008

I2C1_SDA_R
I2C1_SCL_R
TOUCHPAD_INTR#
PTP_DIS#

AFTP6531

TP_VDD → AFTP6529
I2C1_SCL_R → AFTP6528
I2C1_SDA_R → AFTP6527
TOUCHPAD_INTR# → AFTP6525
PTP_DIS# → AFTP6526

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 65 of 106

Main Func = IO Connector

IO DET

[20] IO_DB_DET#_GPPG5

AUDIO

[27,29] AUD_RING
[27,29] AUD_SLEEVE
[28] AUD_HP1_JACK_L1
[28] AUD_HP1_JACK_R1
[27] AUD_SENSE

CRD

[16] CARD1_USB20_N
[16] CARD1_USB20_P
[20] SD_READ_MODE#

USB3.0

PORT1

[16] USB2_USB30_RX_N
[16] USB2_USB30_RX_P
[16] USB2_USB30_TX_N
[16] USB2_USB30_TX_P
[16] USB2_USB20_N
[16] USB2_USB20_P

USB CONTROL

[16] USB_OC1#
[34,35] USB_PWR_EN#

LAN

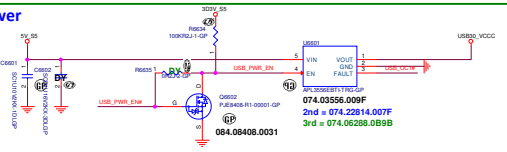
[18] LAN_PCIE_RX_N
[18] LAN_PCIE_RX_P
[18] LAN_PCIE_TX_N
[18] LAN_PCIE_TX_P
[18] LAN_CLK_CPU_N
[18] LAN_CLK_CPU_P
[18] LAN_CLKREQ_CPU_N
[24] PM_LAN_ENABLE
[17,24] PCIE_LAN_WAKE#
[18] LCM_CABLE_DETECT#

FP

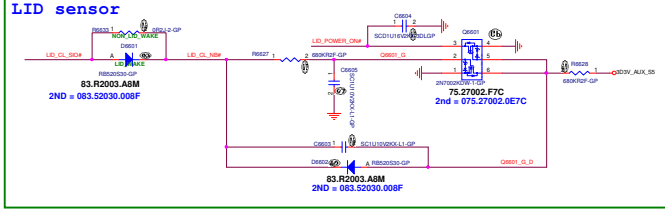
[16] FP1_USB20_N
[16] FP1_USB20_P
[24] FPR_SCAN#
[64] KBC_PWRBTN#_R
[17,40,51] PM_SLP_S4#

[20,24] LID_CL_SIO#
[24] LID_POWER_ON#
[20,24] LID_CL_SIO_TAB#
[17,40,61,62,63,76,91] PLT_RST#
[24,64] LED_MASK#
[20,63] CPU_I2C_SCL_R0
[20,63] CPU_I2C_SDA_R0
[44] PWR_CHG_VBATIN
[55] 3D3V_LCDVDD_R

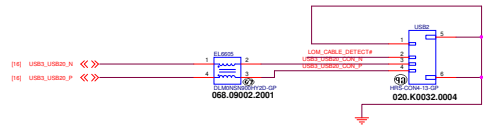
USB2.0 Power



LID sensor



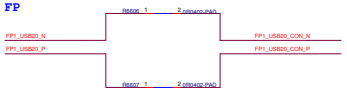
USB2.0 PORT



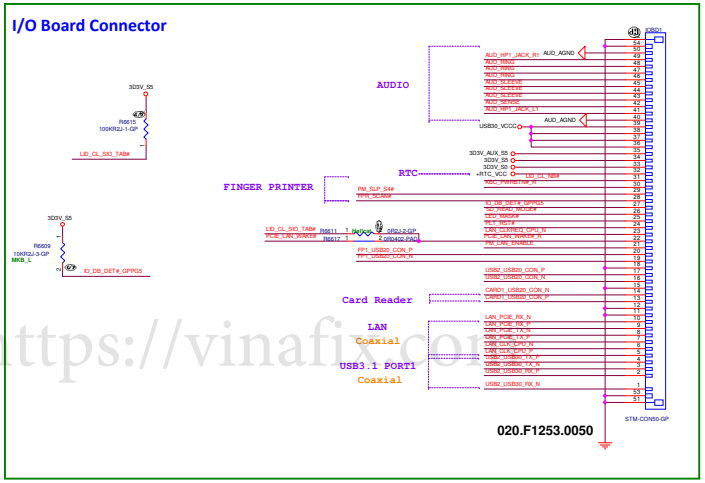
CRD

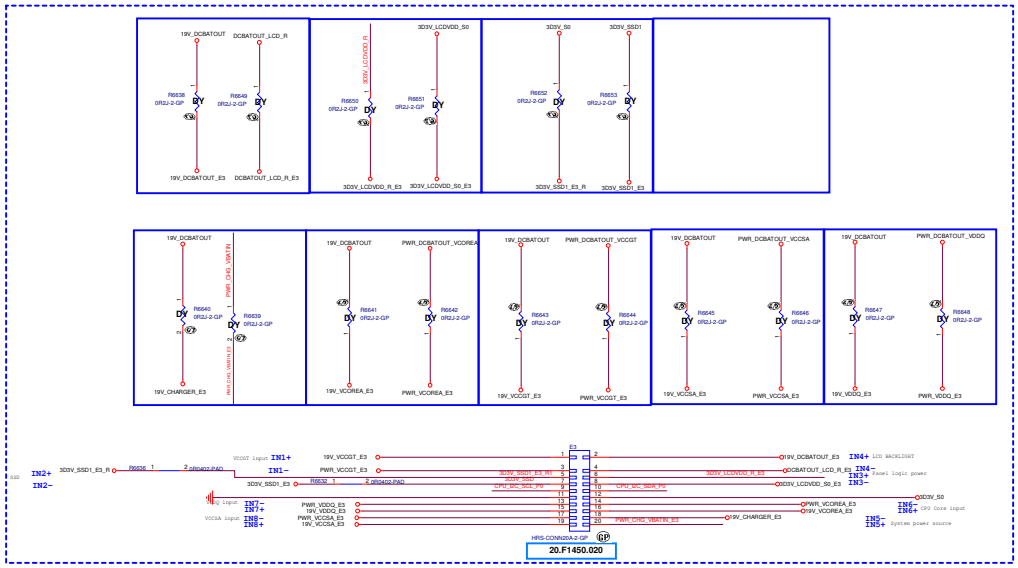
USB3.0 PORT1

FP



I/O Board Connector





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A1	Mockingbird CML	SC

Date: Monday, December 05, 2016 Sheet 68 of 106

Main Func = HALL SENSOR

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 67 of 106

Main Func = Debug

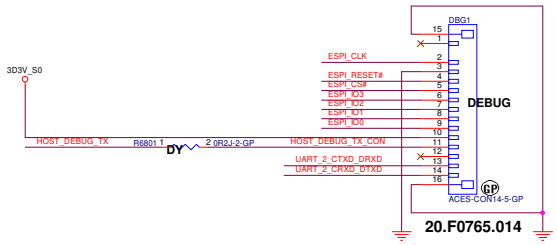
ESPI

[18,24] ESPI_CLK
[18,24] ESPI_RESET#
[18,24] ESPI_CS#
[18,24] ESPI_IO[3..0]
ESPI_IO3
ESPI_IO2
ESPI_IO1
ESPI_IO0

UART

[24] HOST_DEBUG_TX
[20] UART_2_CTXD_DRXD
[20] UART_2_CRXD_DTXD

ESPI Debug Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 68 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Mockingbird CML***	***SC***

Date: Monday, December 09, 2019 Sheet 69 of 106

SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

[20] GSEN2_INT1_C

[20,55] SENSOR_I2C_SCL

[20,55] SENSOR_I2C_SDA

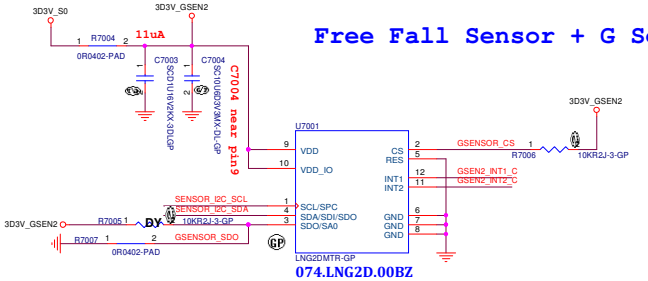
[18] FFS_INT1

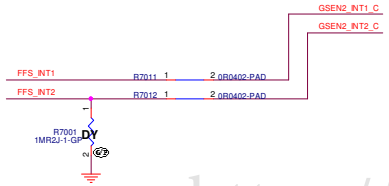
[20] FFS_INT2

[60] FFS_INT2_Q

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

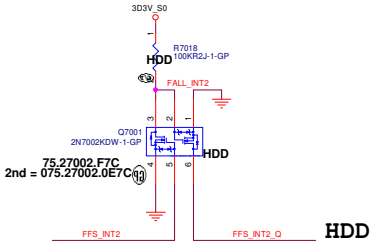
Free Fall Sensor + G Sensor





Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:

(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 70 of 106

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A4	Mockingbird CML	SC

Date: Monday, December 09, 2019 Sheet 71 of 106

Main Func =TI

EC

[74] PD_VBUS_C_CTRL1

[24] UPD1_SMBCLK
[24] UPD1_SMBDAT

[74] VBUS_P_CTRL

[24] CCG5C_I2C_INT#

0513

MUX TUSB546

[73] I2C_DATA_PD
[73] I2C_CLK_PD

[4,73] DP1_HPD_CPU

[73] CCG5_SBU1
[73] CCG5_SBU2

[74] NX5P3363_FO

TYPE-C CONNECTOR

[73] USB1_CC1
[73] USB1_CC2

[73] TOP_MUX_P_L

[73] TOP_MUX_N_L

[73] BOT_MUX_P_L

[73] BOT_MUX_N_L

[73] USB1_SBU1

[73] USB1_SBU2

PCH

[16] USB4_USB20_P
[16] USB4_USB20_N

From System

3D3V_S5

VCC3PD_1

D7202 SBA0520Q-R1-00001-GP-U

For debattery

D7203 SBA0520Q-R1-00001-GP-U

083.00520.0F8F

2nd = 083.05S40.001F

Power

VDDD

C7203 SCD1U16V2KX-3DLGP

C7204 SCD1U16V2KX-3DLGP

C7207 SC1U10V2KX-L1-GP

C7210 SCD1U16V2KX-3DLGP

C7212 SC1U10V2KX-L1-GP

R7217 100KR2J-1-GP

R7223 100KR2J-1-GP

Q7201 2N7002KDW-1-GP

R7218 100KR2J-1-GP

R7222 100KR2J-1-GP

2nd = 075.27002.0E7C

75.27002.F7C

U7201 CYPD5126-40LQXIT-15-GP

074.05126.0S03

C7218 SCD1U16V2KX-3DLGP

C7221 SC330P50V2KX-3-DL-GP

C7220 SC330P50V2KX-3-DL-GP

R7225 10KR2J-3-GP

R7226 10KR2J-3-GP

R7216 10KR2J-3-GP

R7224 0R0402-PAD

R7208 0R0402-PAD

R7207 10KR2F-2-GP

R7209 100KR2J-1-GP

R7221 4K7R2J-L-GP

C7219 SCD1U16V2KX-3DLGP

RN7202 SRN2K2J-1-GP

R7215 2K2R2J-L1-GP

MOD ID Settings

R7201 51KR2J-1-GP

R7213 150KR2J-GP

MOD ID Settings

R7212 100KR2J-1-GP

R7214 100KR2J-1-GP

R7219 1KR2F-3-GP

R7220 1KR2F-3-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB PD(CYPD5126)

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 72 of 108

Main Func = TYPEC MUX

DisplayPort Source

[4] DP2_DDI_TX_P0
[4] DP2_DDI_TX_N0
[4] DP2_DDI_TX_P1
[4] DP2_DDI_TX_N1
[4] DP2_DDI_TX_P2
[4] DP2_DDI_TX_N2
[4] DP2_DDI_TX_P3
[4] DP2_DDI_TX_N3

USB HOST

[16] USB4_USB30_RX_P
[16] USB4_USB30_RX_N
[16] USB4_USB30_TX_P
[16] USB4_USB30_TX_N

DisplayPort AUX

[4] DP2_AUX_CPU_P
[4] DP2_AUX_CPU_N

MUX I2C

[72] I2C_CLK_PD
[72] I2C_DATA_PD

DisplayPort HPD

[4,72] DP1_HPD_CPU

I2C/USB MUX

[72] CCG5_SBU1
[72] CCG5_SBU2

TypeC CC

[72] USB1_SBU1
[72] USB1_SBU2
[72] USB1_CC1
[72] USB1_CC2
[72] TOP_MUX_P_L
[72] TOP_MUX_N_L
[72] BOT_MUX_P_L
[72] BOT_MUX_N_L

For displayport function at dead battery condition

3D3V_SS

3D3V_MUX

R7303 1 — 2 0R0402-PAD

C7329 C7325 C7326 C7327 C7328 C7330 — 0.1UF/25V/X5R-1-GP

3A

0828 EMC

EC7301 — 0.1UF/25V/X5R-1-GP

ED7301 NER20F30NXT5G-GP

083.20F30.008H

20V_VCCPD_VBUS

R7306 10KR2J-3-GP — DY

R7307 4K75R2J-L-GP — DY

CAD_SNK

HPDIN

Slave address : 0X44

U7301

TUSB546-DCIRNQR-1-GP

071.00546.M001

DisplayPort Source

DP2_DDI_TX_P0 C7312 1 — SCD1U16V2KX-3DLGP — DP2_DDI_TX_RE_C_P0 — DP0P
DP2_DDI_TX_N0 C7313 1 — SCD1U16V2KX-3DLGP — DP2_DDI_TX_RE_C_N0 — DP0N
DP2_DDI_TX_P1 C7314 1 — SCD1U16V2KX-3DLGP — DP2_DDI_TX_RE_C_P1 — DP1P
DP2_DDI_TX_N1 C7307 1 — SCD1U16V2KX-3DLGP — DP2_DDI_TX_RE_C_N1 — DP1N
DP2_DDI_TX_P2 C7309 1 — SCD1U16V2KX-3DLGP — DP2_DDI_TX_RE_C_P2 — DP2P
DP2_DDI_TX_N2 C7308 1 — SCD1U16V2KX-3DLGP — DP2_DDI_TX_RE_C_N2 — DP2N
DP2_DDI_TX_P3 C7311 1 — SCD1U16V2KX-3DLGP — DP2_DDI_TX_RE_C_P3 — DP3P
DP2_DDI_TX_N3 C7310 1 — SCD1U16V2KX-3DLGP — DP2_DDI_TX_RE_C_N3 — DP3N

USB1_SSRX_C_P1 — RX1P
USB1_SSRX_C_N1 — RX1N
USB1_SSRX_C_P2 — RX2P
USB1_SSRX_C_N2 — RX2N
USB1_SSTX_C_P1 — TX1P
USB1_SSTX_C_N1 — TX1N
USB1_SSTX_C_P2 — TX2P
USB1_SSTX_C_N2 — TX2N

USB HOST

USB4_USB30_RX_P C7305 1 — SCD1U16V2KX-3DLGP — USB4_USB30_RX_C_P — SSRXP
USB4_USB30_RX_N C7306 1 — SCD1U16V2KX-3DLGP — USB4_USB30_RX_C_N — SSRXN
USB4_USB30_TX_P C7303 1 — SCD1U16V2KX-3DLGP — USB4_USB30_TX_C_P — SSTXP
USB4_USB30_TX_N C7304 1 — SCD1U16V2KX-3DLGP — USB4_USB30_TX_C_N — SSTXN

3D3V_MUX

R7301 1 — 100KR2J-1-GP — DP2_AUX_C_N
R7302 1 — 100KR2J-1-GP — DP2_AUX_C_P

EQ0 EQ1 EQ2 EQ3 EQ4 EQ5 EQ6 — HPDIN — CAD_SNK — I2CEN — CCG5_SBU1 — CCG5_SBU2 — DP2_AUX_C_P — DP2_AUX_C_N — DPEQ0_A1 — DPEQ1 — SSEQ0_A0 — SSEQ1 — I2C_CLK_PD_MUX — I2C_DATA_PD_MUX — MUX_HPD_PD

R7320 R7318 R7344 R7325 R7341 R7327 R7323 — 1KR2J-1-GP — DY
R7321 R7319 R7343 R7340 R7342 R7322 R7324 — 1KR2J-1-GP

FLIP PORT	CTL2 PARITY	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

DCI	Note DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode

Note DCI	
DP Enable in GPIO mode Unused in I2C mode	
AUX Snoop EN in GPIO mode EN in I2C mode	
HPD	

20V_VCCPD_VBUS

USB1

USB1_SSTX_CON_P1 — A1 GND — B1 GND
USB1_SSTX_CON_N1 — A2 SSTXP1 — B2 SSTXP2 — USB1_SSTX_CON_P2
A3 SSTXN1 — B3 SSTXN2 — USB1_SSTX_CON_N2
USB1_CC1 — A4 VBUS#A4 — B4 VBUS#B4
TOP_MUX_P — A5 CC1 — B5 CC2 — USB1_CC2
TOP_MUX_N — A6 DP1 — B6 DP2 — BOT_MUX_P
A7 DN1 — B7 DN2 — BOT_MUX_N
USB1_SBU1 — A8 RFU1 — B8 RFU2 — USB1_SBU2
USB1_SSRX_CON_N2 — A9 VBUS#A9 — B9 VBUS#B9 — USB1_SSRX_CON_N1
USB1_SSRX_CON_P2 — A11 SSRXN2 — B11 SSRXN1 — USB1_SSRX_CON_P1
A12 SSRXP2 — B12 SSRXP1
GND — GND

R7308 2 — 1 USB1_SBU1 — 1 R7309 — 2 20K0F-GP

SKT-USB28-1-GP

062.10009.0681

CHASSIS#13 CHASSIS#14 CHASSIS#15 CHASSIS#16

USB1_SSTX_C_P1 C7324 1 — SCD1U16V2KX-3DLGP — USB1_SSTX_CMC_P1 — R7310 1 — 2 0R0402-PAD — USB1_SSTX_CON_P1

USB1_SSTX_C_N1 C7323 1 — SCD1U16V2KX-3DLGP — USB1_SSTX_CMC_N1 — R7311 1 — 2 0R0402-PAD — USB1_SSTX_CON_N1

ED7302 — AZ1043-04F-R7G-GP

075.01043.0073

USB1_SSRX_C_P1 C7331 1 — SCD33U6D3V2KX-3-GP — USB1_SSRX_CMC_P1 — R7312 1 — 2 0R0402-PAD — USB1_SSRX_CON_P1

USB1_SSRX_C_N1 C7332 1 — SCD33U6D3V2KX-3-GP — USB1_SSRX_CMC_N1 — R7313 1 — 2 0R0402-PAD — USB1_SSRX_CON_N1

ED7308 — AZ1043-04F-R7G-GP

075.01043.0073

USB1_SSRX_C_P2 C7333 1 — SCD33U6D3V2KX-3-GP — USB1_SSRX_CMC_P2 — R7314 1 — 2 0R0402-PAD — USB1_SSRX_CON_P2

USB1_SSRX_C_N2 C7334 1 — SCD33U6D3V2KX-3-GP — USB1_SSRX_CMC_N2 — R7315 1 — 2 0R0402-PAD — USB1_SSRX_CON_N2

USB1_SSTX_C_P2 C7321 1 — SCD1U16V2KX-3DLGP — USB1_SSTX_CMC_P2 — R7316 1 — 2 0R0402-PAD — USB1_SSTX_CON_P2

USB1_SSTX_C_N2 C7322 1 — SCD1U16V2KX-3DLGP — USB1_SSTX_CMC_N2 — R7317 1 — 2 0R0402-PAD — USB1_SSTX_CON_N2

0614 Layout HT

ED7304 — BOT_MUX_P — BOT_MUX_N — AZ5315-02F-GP — 83.05315.0A0

ED7305 — USB1_SBU1 — USB1_SBU2 — AZ5315-02F-GP — 83.05315.0A0

ED7306 — TOP_MUX_P — TOP_MUX_N — AZ5315-02F-GP — 83.05315.0A0

ED7307 — USB1_CC1 — USB1_CC2 — AZ5315-02F-GP — 83.05315.0A0

USB1_SSRX_CON_P1 — R7345 — 0R0402-PAD
USB1_SSRX_CON_N1 — R7346 — 0R0402-PAD
USB1_SSRX_CON_P2 — R7347 — 0R0402-PAD
USB1_SSRX_CON_N2 — R7348 — 0R0402-PAD

TOP_MUX_N_L — EL7301 — TOP_MUX_N
TOP_MUX_P_L — TOP_MUX_P

068.09002.2001

DLM05N900HYZD-GP

BOT_MUX_P_L — EL7302 — BOT_MUX_P
BOT_MUX_N_L — BOT_MUX_N

068.09002.2001

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Title: USB Type-C&MUX(TUSB546)

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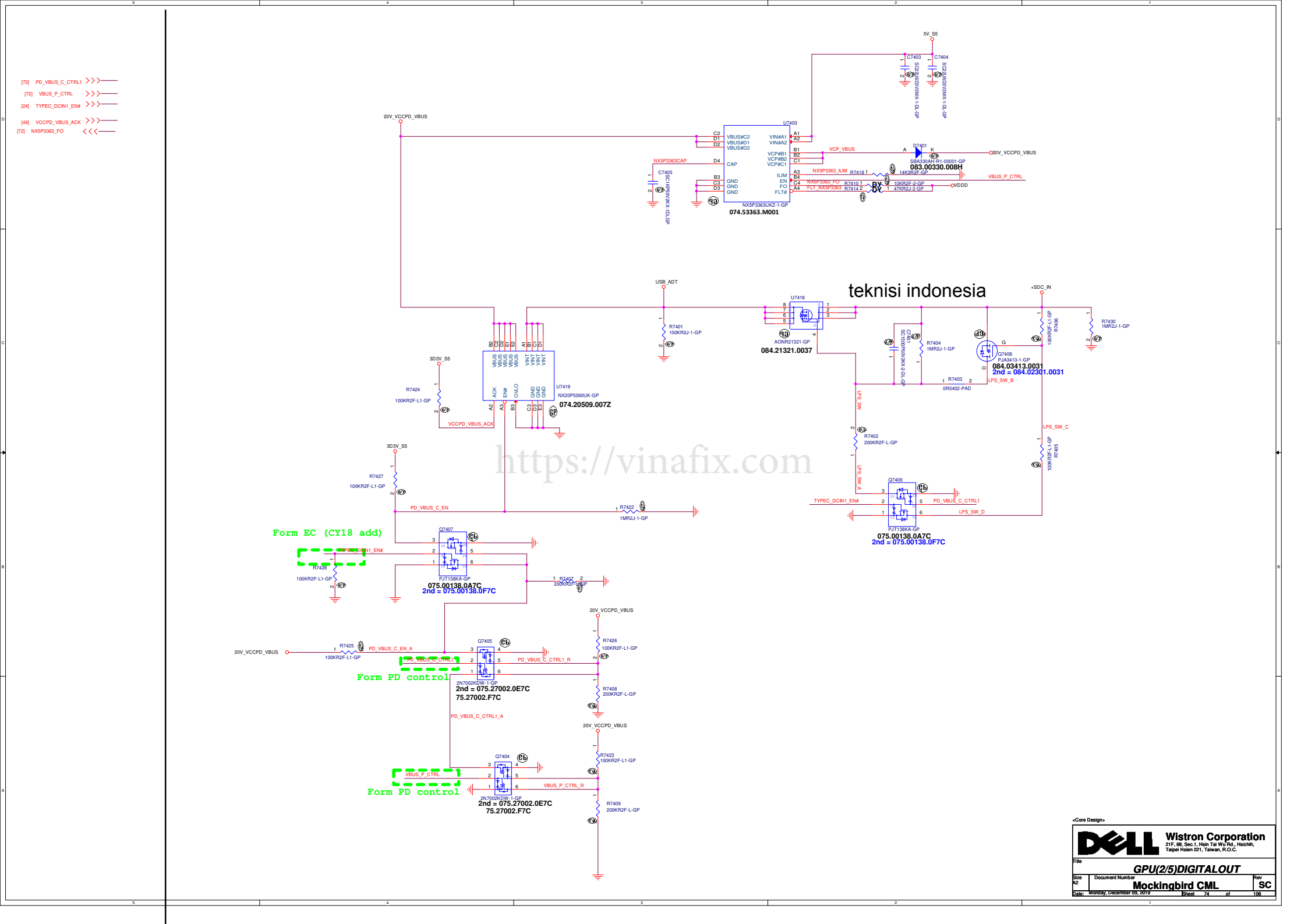
Date: Monday, December 09, 2019 | Sheet 73 of 108



<Core Design>

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Title: GPU(2/5)DIGITALOUT

Size: A2 | Document Number: Mockingbird CML | Rev: SC

Date: Monday, December 09, 2019 | Sheet 74 of 106

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Mockingbird CML* | Rev: *SC*

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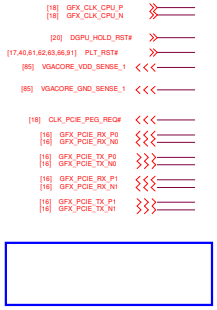
Main Func = dGPU



0508

dGPU Reset

73.01G08.EHG
2ND = 073.17S08.000G
3RD = 73.01G08.LD4

084.08408.0031

071.0N17S.0000

1.05V +/- 30mV
3.3A

Place close VDD ball

Place close Chip

3.3V +/- 5%
210mA

POWER IC

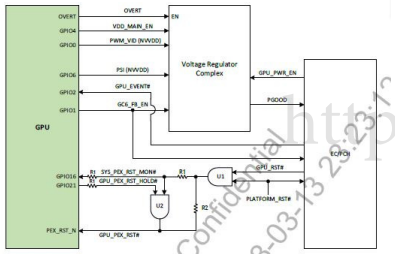


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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GPU(1/5)PEG

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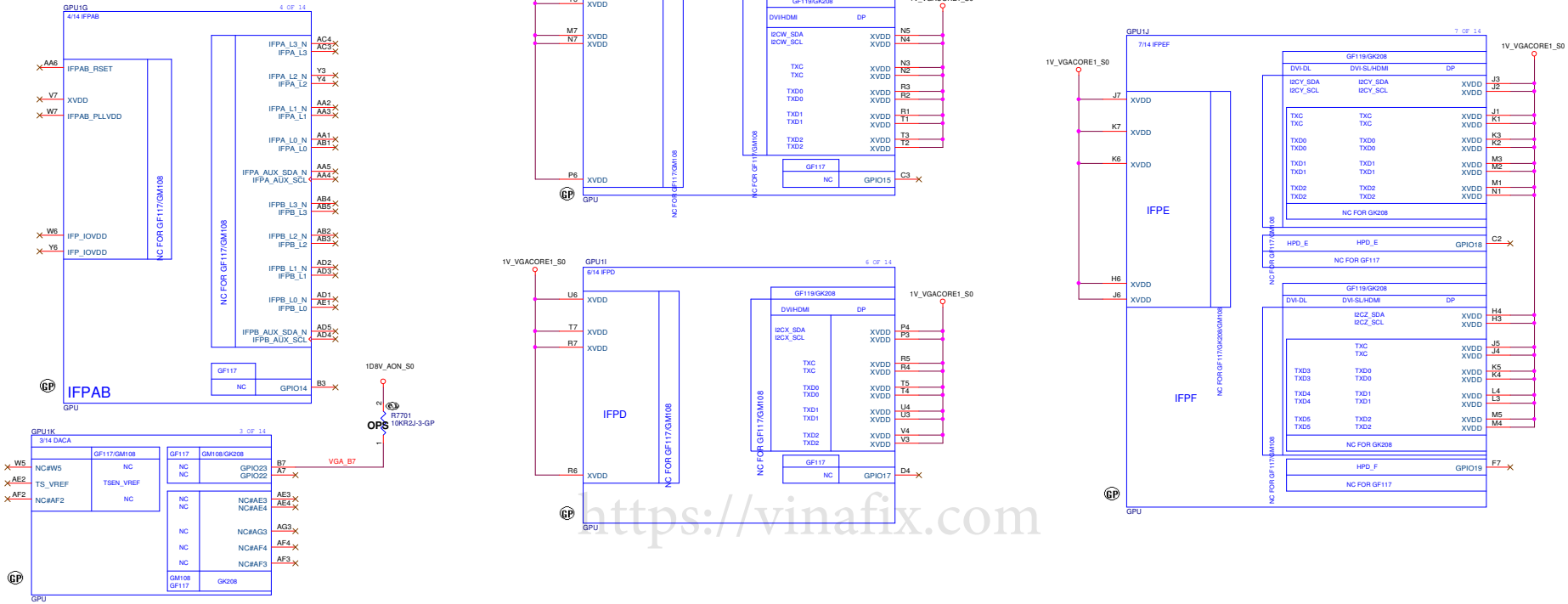
Main Func = dGPU



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Title: GPU(2/5)DIGITALOUT

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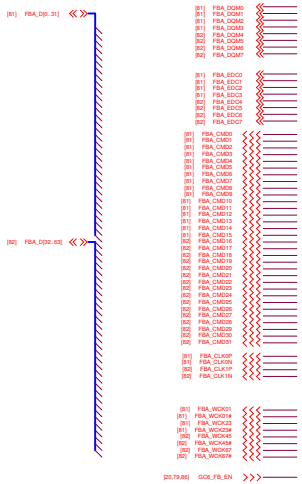
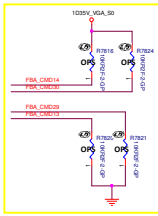
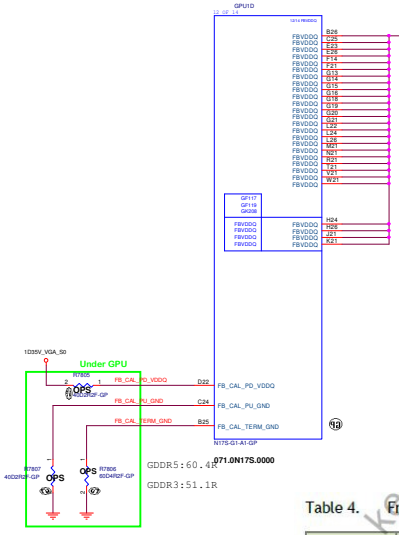
Main Func = dGPU



Modify by change to GDDR5



Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5



GDDR5:60.4R
GDDR3:51.1R

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type				
	30 Ω (ESR=0.010 Ω)	0603	1	1	Near GPU

Main Func = dGPU

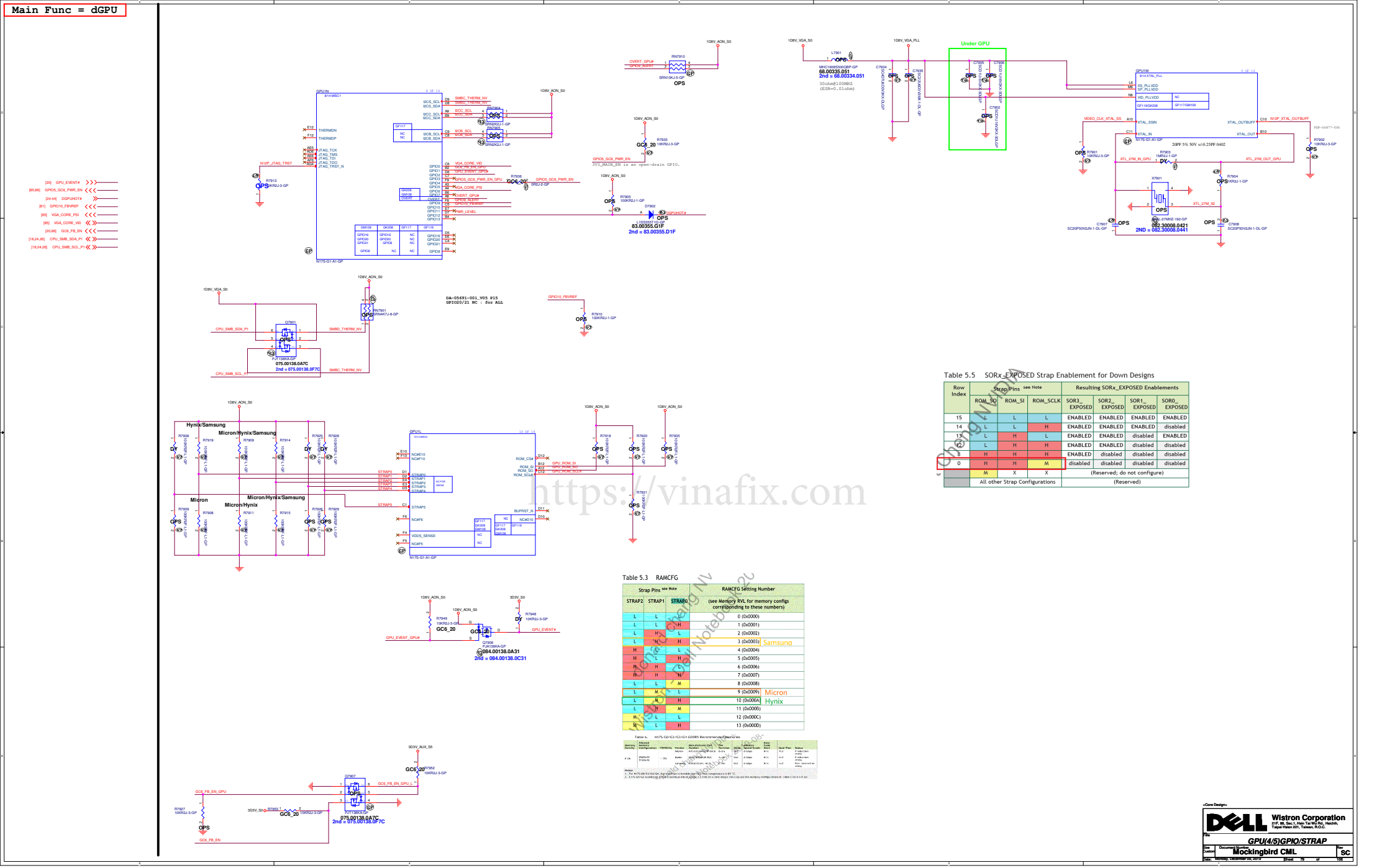


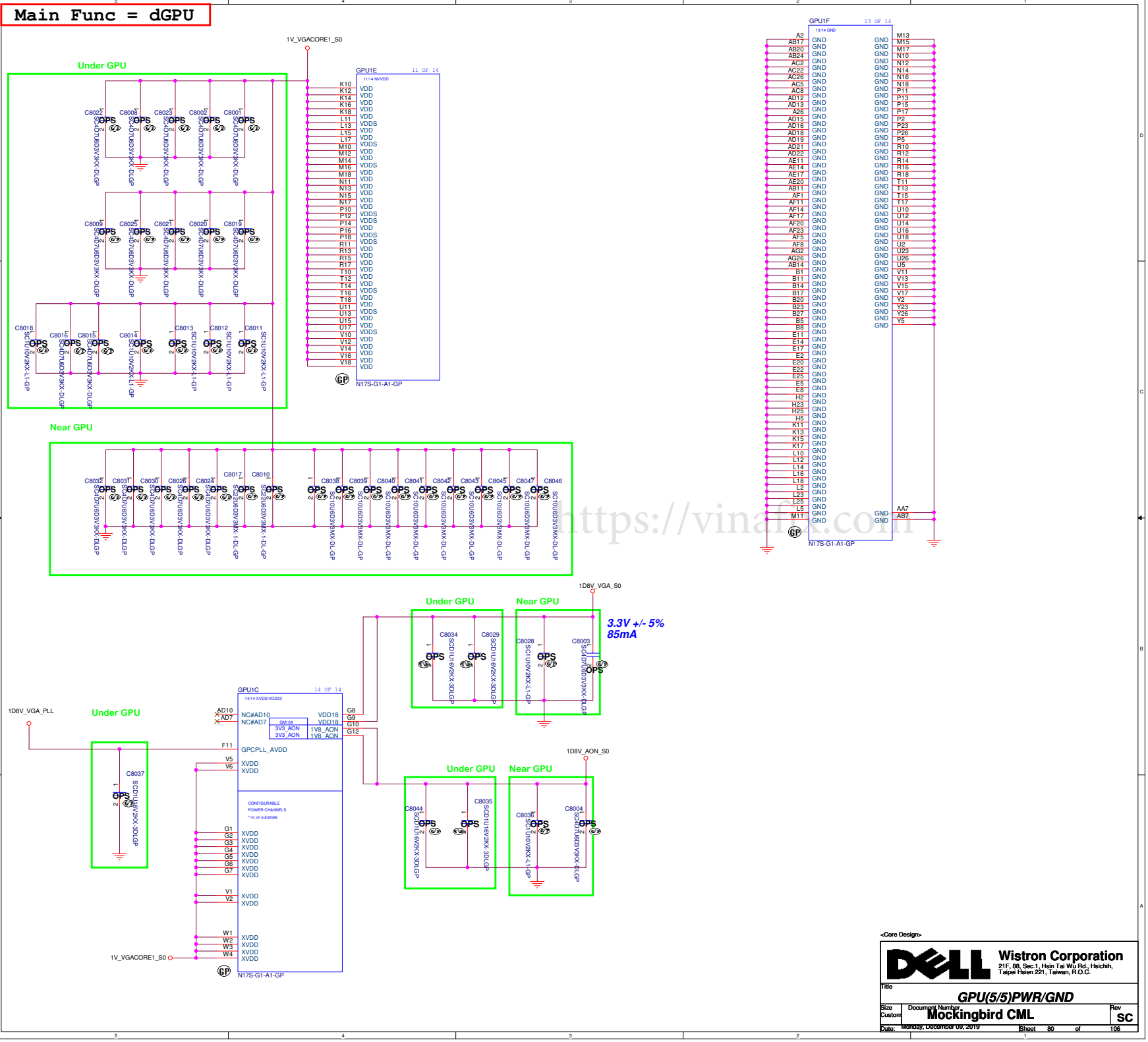
Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)	
STRAP2	STRAP1	STRAP0		
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	Samsung
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	Micron
L	M	H	10 (0x000A)	Hynix
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

Main Func = dGPU



<Core Design>

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Title: GPU(5/5)PWR/GND

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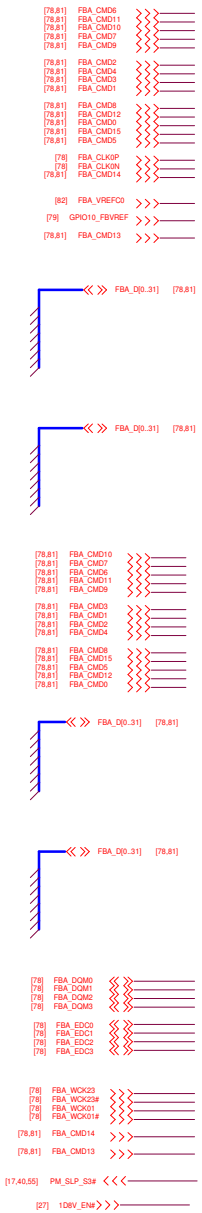
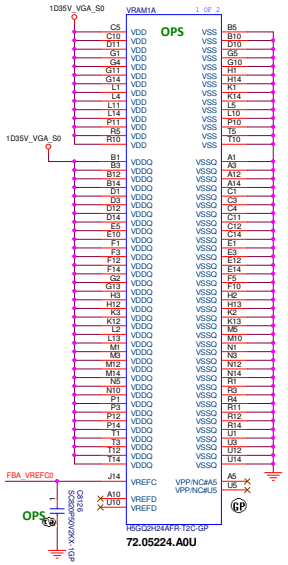
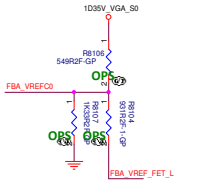
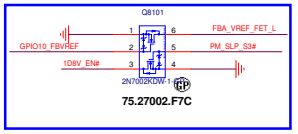
SSID = VRAM





Frame Buffer Patition A-Lower Half





FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

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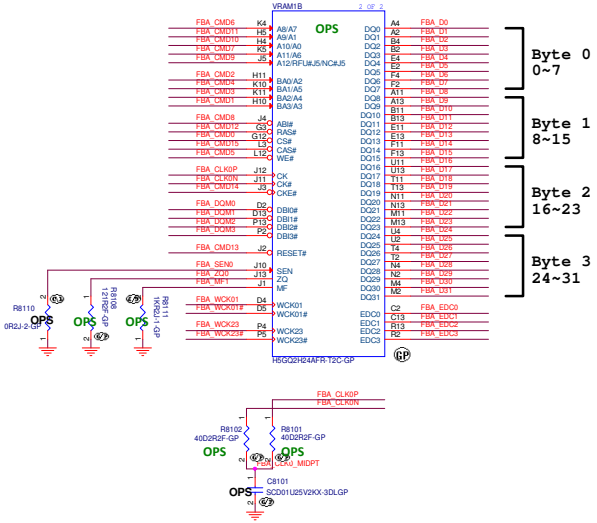
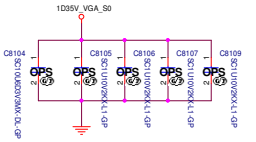
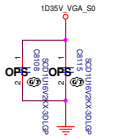
Normal(MF=0)



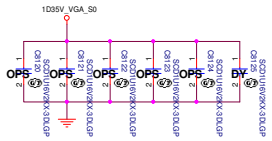
Place close VDD ball



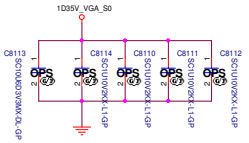
Place close VDD ball



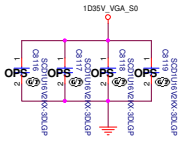
Place close VDD ball



Place close VDDQ ball



Place close VDDQ ball



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Title: GPU-VRAM1,2 (1/4)

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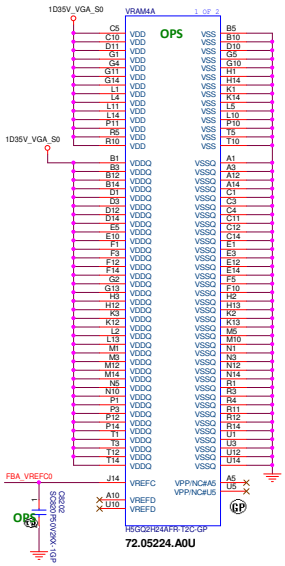
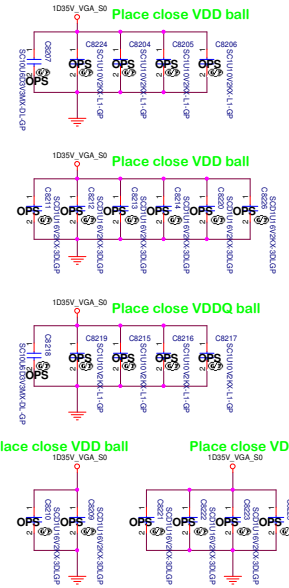
SSID = VRAM

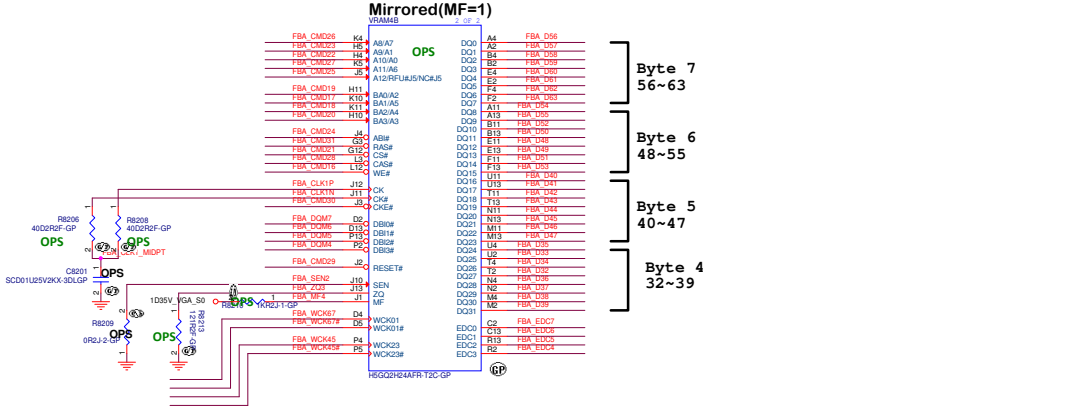
Frame Buffer Patition A-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low





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Title

GPU-VRAM5,6 (3/4)

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Title

GPU-VRAM7,8 (4/4)

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RT8816B For NVVDDS

OFFPAGE-Signal

PH on EE side

1. Check EE side
2. Modify DAT

PH on EE side

EE need check

Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

2nd = 73.R2G08.DAH
3rd = 73.01G06.DHG

For VGA_CORE sequence
EE need check

2nd = 075.00138.0F7C

2nd = 084.27002.0N31

OFFPAGE-GAP

Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

teknisi indonesia

VGA : N17S-G3/G4 / NVVDDS
EDP-Continuous : 28.6A
EDP-Peak : 60.3A

ID:31/54A ,
Rdson: 6.8~8.6/2.8~3.5m (Q1/Q2)
1st = 075.07321.0072

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 37A , Isat : 41A

OCP setting
133K ohm for OCP around 84.42A setting

SS setting

Place Near GPU (NVVDD5)
1X330uF (Poscap) - PT8511 (Page85)

074.08816.0A73

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Title: GPU (RT8816B_VGA)
Size: A1 | Document Number: Mockingbird CML | Rev: SC
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Main Func = dGPU

Main Func = dGPU

[Dd-07159-001 Rev03]Power up sequence:
3.3V ==> MVVDD (VGA_CORE) ==> PEX_VDD (1.05V) ==> FBVDD/Q (1.35V)

3D3V_S0 to 3V3_AON_S0 and 3D3V_VGA_S0

dGPU Power Discharge Circuit

1V_VGA_S0

VGA_CORE

1D35V_VGA_S0

1D8V_AON_S0

1D8V_AON_S0 to 1D8V_VGA_S0

1D8V_VGA_S0

RT5797 for 1V_VGA_S0

For tuning VGA_CORE sequence.

1V_VGA_S0
Design Current=0.1A

1D35V_VGA_S0

SY8288RAC for 1D35V

OCP setting	
High	16A
Float	12A
Low	8A

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DISCRETE VGA POWER

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Main Func = dGPU

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Title

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Main Func = UnusedParts

H1 HOLE256R142-1-GP — ZZ.PAD01.V91

H2 HOLE — ZZ.0HOLE.XXX — 20190902

H5 HOLE335R178-GP — ZZ.00PAD.7F1

HS1 STF237R113H91-GP — 434.0HH0K.0001

GPU/CPU SKREW HOLE

H7 HOLE276R150-GP — ZZ.00PAD.H91
H8 HOLE276R150-GP — ZZ.00PAD.H91
H9 HOLE276R150-GP — ZZ.00PAD.H91
H10 HOLE276R150-GP — ZZ.00PAD.H91
H11 HOLE276R154-GP — ZZ.00PAD.2T1
H12 HOLE276R154-GP — ZZ.00PAD.2T1
H13 HOLE276R154-GP — ZZ.00PAD.2T1

TYPEC SKREW HOLE

H14 HOLE256R142-1-GP — ZZ.PAD01.V91
H15 HOLE256R142-1-GP — ZZ.PAD01.V91

HDMI SKREW HOLE

For acoustic noice

Main Func = EMI Capacitors

Mind the voltage rating of the caps.

19V_DCBATOUT — EC8917 SC1KP50V2KX-1DLGP, EC8919 SC1KP50V2KX-1DLGP, EC8925 SC1KP50V2KX-1DLGP, EC8915 SC1KP50V2KX-1DLGP, EC8928 SC1KP50V2KX-1DLGP, EC8929 SC1KP50V2KX-1DLGP

[43,44] +DC_IN_C — EC8958 SCD1U25V2KX-1DLGP

X02 20190412

19V_DCBATOUT — EC8957 SC1KP50V2KX-1DLGP, EC8962 SCD1U25V2KX-1DLGP, EC8963 SC1KP50V2KX-1DLGP

X02 20190412

+SDC_IN — EC8969 SCD1U25V2KX-1DLGP, EC8970 SCD1U25V2KX-1DLGP, EC8971 SCD1U25V2KX-1DLGP, EC8972 SC1U25V2KX-4GP, EC8973 SCD1U25V2KX-1DLGP, EC8974 SCD1U25V2KX-1DLGP

1V_CPU_CORE — EC8975 SCD1U16V2KX-3DLGP, EC8976 SCD1U16V2KX-3DLGP, EC8977 SCD1U16V2KX-3DLGP

1V_VCCGT — EC8978 SCD1U16V2KX-3DLGP, EC8979 SCD1U16V2KX-3DLGP

1V_VCCSA — EC8980 SCD1U16V2KX-3DLGP, EC8981 SCD1U16V2KX-3DLGP

1D2V_S3 — EC8901 SC1U16V2KX-1DLGP, EC8902 SC1U16V2KX-1DLGP, EC8903 SC1U16V2KX-1DLGP, EC8904 SC1U16V2KX-1DLGP, EC8905 SC1U16V2KX-1DLGP, EC8906 SC1U16V2KX-1DLGP, EC8907 SC1U16V2KX-1DLGP, EC8908 SC1U16V2KX-1DLGP

X02 20190412

3D3V_S0 — EC8950 SCD1U10V2KX-1GP, EC8951 SCD1U10V2KX-1GP, EC8952 SCD1U10V2KX-1GP, EC8953 SCD1U10V2KX-1GP, EC8954 SCD1U16V2KX-3DLGP, EC8955 SCD1U16V2KX-3DLGP, EC8956 SCD1U16V2KX-3DLGP, EC8959 SCD1U16V2KX-3DLGP, EC8960 SCD1U16V2KX-3DLGP, EC8964 SCD1U16V2KX-3DLGP

PWR_DCBATOUT_VCOREA — EC8909 SC1KP50V2KX-1DLGP, EC8910 SC1KP50V2KX-1DLGP, EC8911 SC1KP50V2KX-1DLGP, EC8912 SC1KP50V2KX-1DLGP

X02 20190412

PWR_DCBATOUT_VCCGT — EC8913 SC1KP50V2KX-1DLGP, EC8914 SC1KP50V2KX-1DLGP

X02 20190412

5V_S0 — EC8933 SCD1U10V2KX-1GP, EC8934 SCD1U10V2KX-1GP, EC8935 SCD1U10V2KX-1GP, EC8936 SCD1U10V2KX-1GP, EC8937 SCD1U10V2KX-1GP, EC8938 SCD1U10V2KX-1GP, EC8939 SCD1U10V2KX-1GP

5V_S5 — EC8947 SCD1U10V2KX-1GP, EC8948 SCD1U10V2KX-1GP, EC8949 SCD1U10V2KX-1GP

1V_VGACORE1_S0 — EC8961 SCD1U16V2KX-3DLGP, EC8965 SCD1U16V2KX-3DLGP, EC8966 SCD1U16V2KX-3DLGP, EC8967 SCD1U16V2KX-3DLGP, EC8968 SCD1U16V2KX-3DLGP

PWR_DCBATOUT_VCOREA — EC8982 SCD1U25V2KX-1DLGP, EC8983 SCD1U25V2KX-1DLGP

優先放在PC4705旁邊
或相對PC4705的Top層

PWR_DCBATOUT_VCCGT — EC8984 SCD1U25V2KX-1DLGP

優先放在PC4717旁邊
或相對PC4717的Top層

PWR_DCBATOUT_VDDQ — EC8985 SCD1U25V2KX-1DLGP

優先放在PC4804旁邊
或相對PC4804的Top層

20V_DCBATOUT — EC8986 SCD1U25V2KX-1DLGP

PWR_DCBATOUT_1D35V — EC8987 SCD1U25V2KX-1DLGP

Main Func = RF Capacitors

Mind the voltage rating of the caps.

5V_S5 — 0.1uF 0402 x 8 — FC8906 SCD1U16V2KX-3DLGP, FC8907 SCD1U16V2KX-3DLGP, FC8908 SC1U10V2KX-1GP, FC8909 SCD1U16V2KX-3DLGP, FC8940 SCD1U16V2KX-3DLGP, FC8941 SCD1U16V2KX-3DLGP, FC8942 SCD1U16V2KX-3DLGP, FC8943 SC1U10V2KX-1GP

19V_DCBATOUT — 0.1uF 0402 x 8 — FC8916 SC1U25V2KX-4GP, FC8917 SC1U25V2KX-4GP, FC8918 SC1U25V2KX-4GP, FC8920 SCD1U25V2KX-1DLGP, FC8921 SC1U25V2KX-4GP, FC8922 SC1U25V2KX-4GP, FC8923 SC1U25V2KX-4GP, FC8924 SC1U25V2KX-4GP

3D3V_S5 — 0.1uF 0402 x 8 — FC8901 SCD1U16V2KX-3DLGP, FC8903 SCD1U16V2KX-3DLGP, FC8904 SCD1U16V2KX-3DLGP, FC8905 SCD1U16V2KX-3DLGP, FC8936 SCD1U16V2KX-3DLGP, FC8937 SCD1U16V2KX-3DLGP, FC8938 SCD1U16V2KX-3DLGP, FC8939 SC1U10V2KX-1GP

1D05V_S5 — 0.1uF 0402 x 8 — FC8911 SCD1U16V2KX-3DLGP, FC8912 SCD1U16V2KX-3DLGP, FC8913 SC1U10V2KX-1GP, FC8914 SCD1U16V2KX-3DLGP, FC8944 SCD1U16V2KX-3DLGP, FC8945 SCD1U16V2KX-3DLGP, FC8946 SCD1U16V2KX-3DLGP, FC8947 SCD1U16V2KX-3DLGP

3D3V_S0 — 0.1uF 0402 x 6 — FC8948 SC1U10V2KX-1GP, FC8949 SCD1U16V2KX-3DLGP, FC8950 SCD1U16V2KX-3DLGP, FC8951 SCD1U16V2KX-3DLGP, FC8952 SCD1U16V2KX-3DLGP, FC8954 SCD1U16V2KX-3DLGP

1D2V_S3 — 0.1uF 0402 x 3 — FC8955 SCD1U16V2KX-3DLGP, FC8956 SCD1U16V2KX-3DLGP, FC8958 SCD1U16V2KX-3DLGP

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Title: UNUSED PARTS/EMI Capacitors

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Title

Reserved

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Main Func = TPM

[17,40,61,62,63,66,76] PLT_RST#

[18,24,25] SPI_CLK_ROM
[15,18,24,25] SPI_SI_ROM
[18,24,25] SPI_SO_ROM
[18] SPI_CS_ROM_N2

[20] PIRQA#

[18] TPM_SPI_IRQ#

3D3V_S5 R9149 0R2J-2-GP
DY ST_TPM
3D3V_S0 R9150 TPM 0R2J-2-GP 3D3V_TPM

3D3V_TPM
TPM C9109 SC10U6D3V3MX-DL-GP
TPM C9112 SCD1U16V2KX-3DLGP
TPM C9113 SCD1U16V2KX-3DLGP

3D3V_S5_PCH
R9148 10KR2J-3-GP TPM SPI_CS2#_IC

3D3V_TPM
R9151 10KR2J-3-GP TPM
R9124 DY 0R2J-2-GP TPM_SPI_IRQ#
SPI_IRQ#_TPM2 R9123 TPM 0R2J-2-GP PIRQA#

3D3V_TPM 5mA
TPM C9104 SCD1U16V2KX-3DLGP

3D3V_S5 40mA
TPM C9106 SC10U6D3V3MX-DL-GP
TPM C9108 SCD1U16V2KX-3DLGP

SPI_SI_ROM R9133 TPM 15R2J-GP SPI_SI_ROM_TPM
SPI_SO_ROM R9132 TPM 15R2J-GP SPI_SO_ROM_TPM
SPI_CS_ROM_N2 R9130 TPM 0R2J-2-GP SPI_CS2#_IC
SPI_CLK_ROM R9138 TPM 15R2J-GP SPI_CLK_ROM_TPM
Close to U2501

PLT_RST#

U9101_2_GND
R9152 0R2J-2-GP
DY ST_TPM

U9101 TPM
8 VHIO
22 VHIO
1 VSB
21 MOSI/GPIO7
24 MISO
20 SCS#/GPIO5
19 SCLK
17 PLTRST#
16 GND
23 GND
33 GND
2 NC#2
3 NC#3
5 NC#5
29 SDA/GPIO0 TPM_GPIO0 TP9101
30 SCL/GPIO1 TPM_GPIO1 TP9102
18 PIRQ#/GPIO2 SPI_IRQ#_TPM2
6 GPIO3 TPM_GPIO3 TP9103
13 GPIO4 TPM_GPIO4 R9118 DY 2K2R2F-GP SPI_CS_ROM_N2
4 PP/GPIO6 TPM_GPIO6_PP TP9104
7 NC#7
9 NC#9
10 NC#10
11 NC#11
12 NC#12
14 NC#14
15 NC#15
25 NC#25
26 NC#26
27 NC#27
28 NC#28
31 NC#31
32 NC#32
NPCT750JAAYX-1-GP
071.00750.M001

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Title: INT IO (TPM)

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SSID = Finger Print

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Title: Finger Print

Size	Document Number	Rev
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Size: A3 | Document Number: *Mockingbird CML* | Rev: *SC*

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Title

LVDS_Switch

Size	Document Number	Rev
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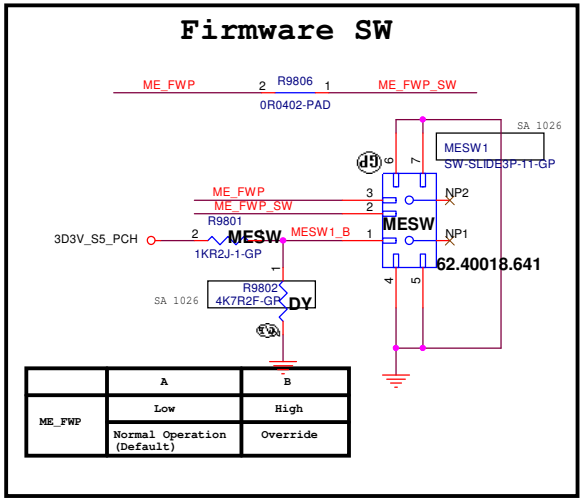
Main Func = Firmware SW

[19] ME_FWP_SW
[24] ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

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Title: CRT_Switch

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Title

Debug (XDP debug)

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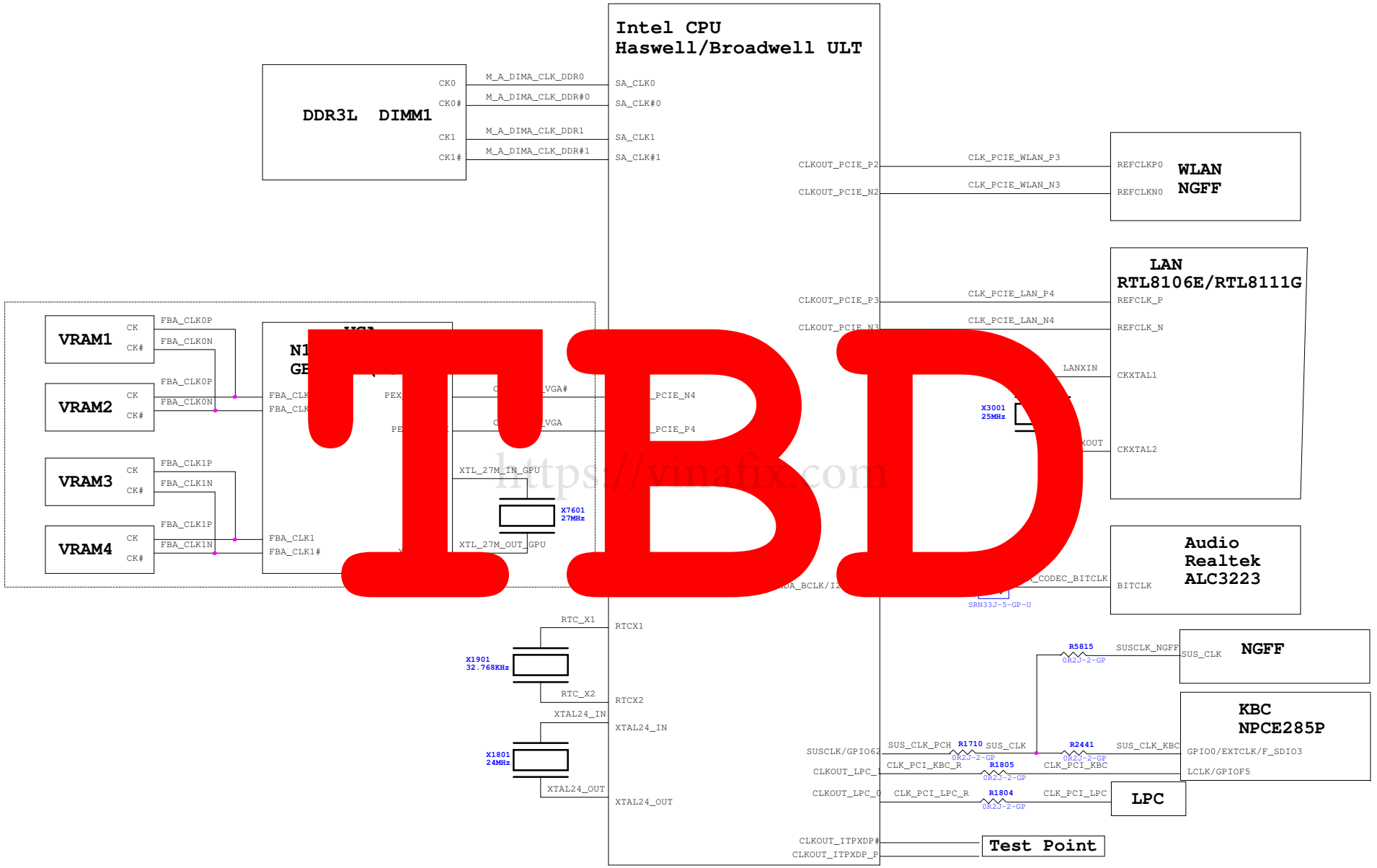
CLK Block Diagram



TBD

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Title: CLK Block Diagram

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Change notes –

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: *Change History*

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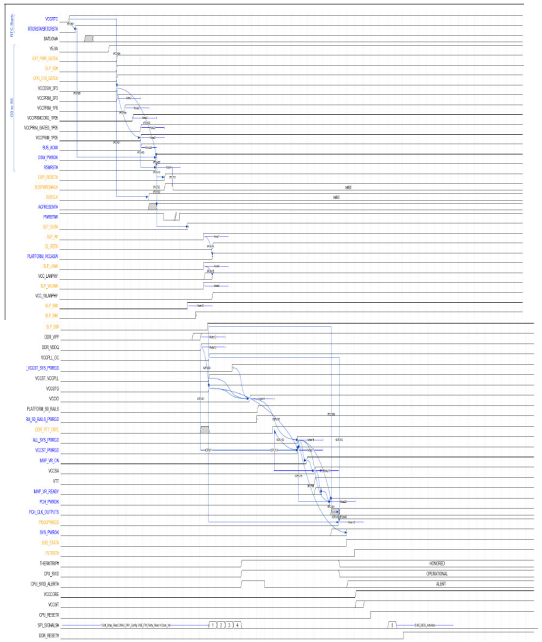
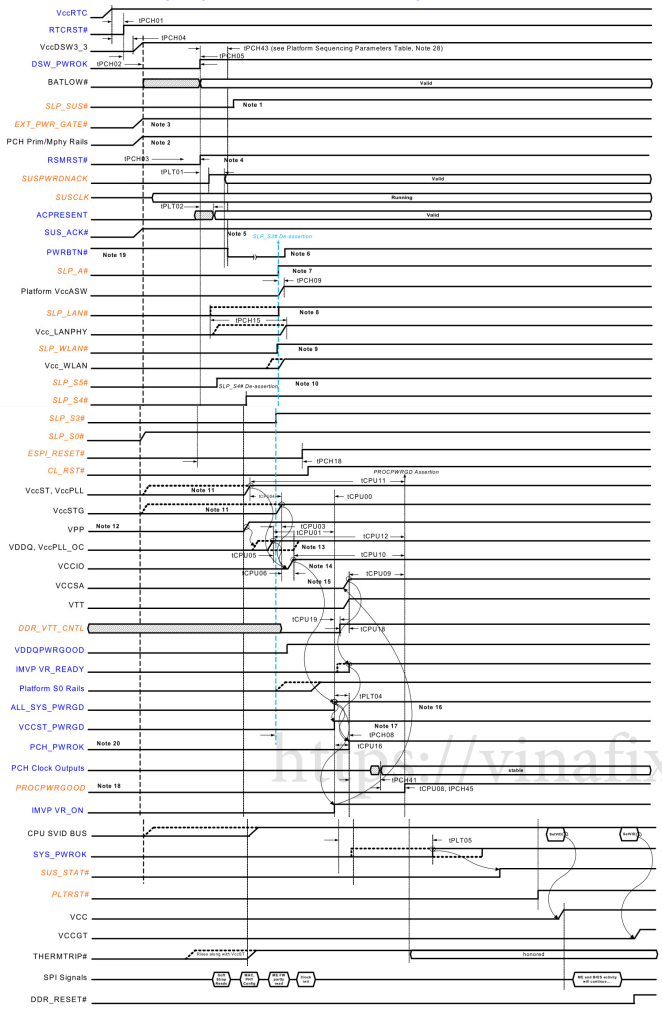
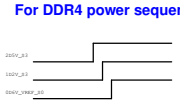
Figure 12-19.WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



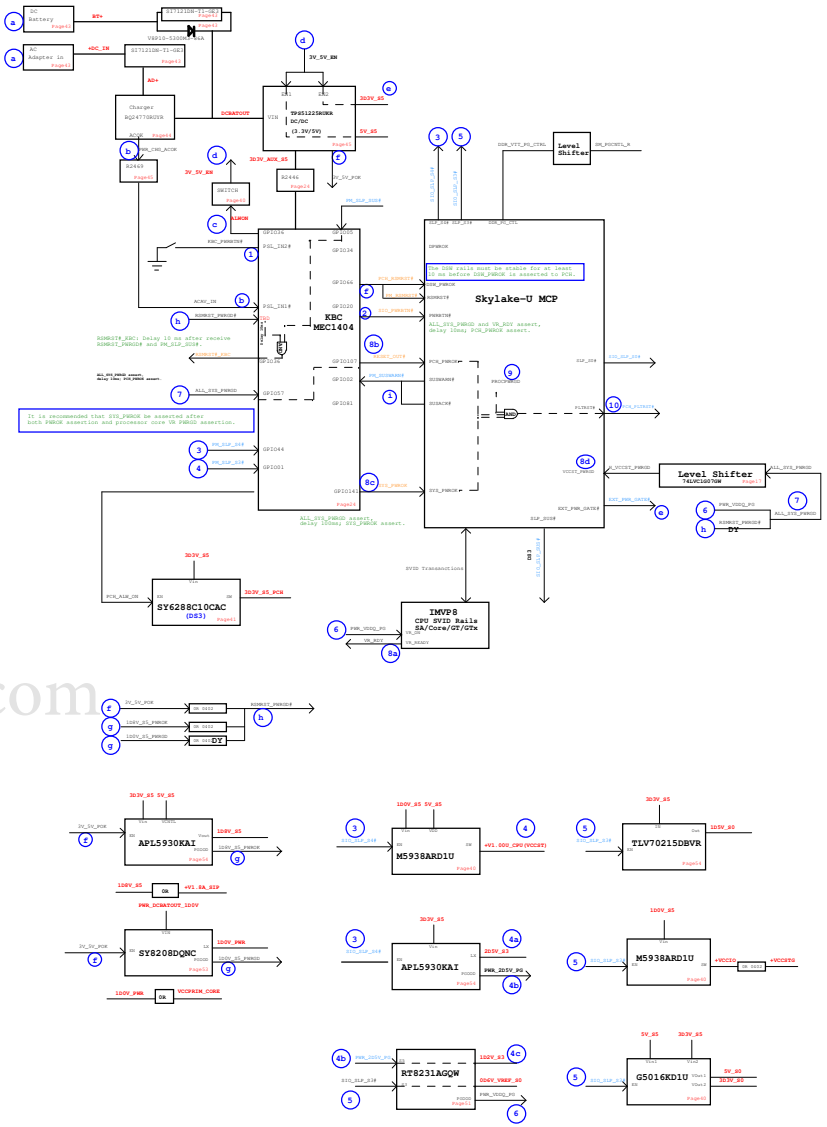
KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



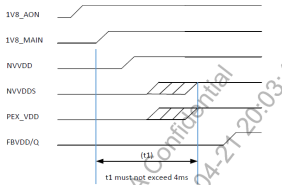
For DDR4 power sequence



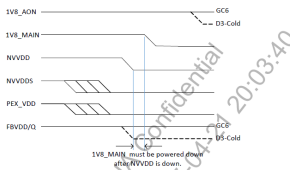
Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



NV N17S GPU Power ON sequence



NV N17S GPU Power Down sequence



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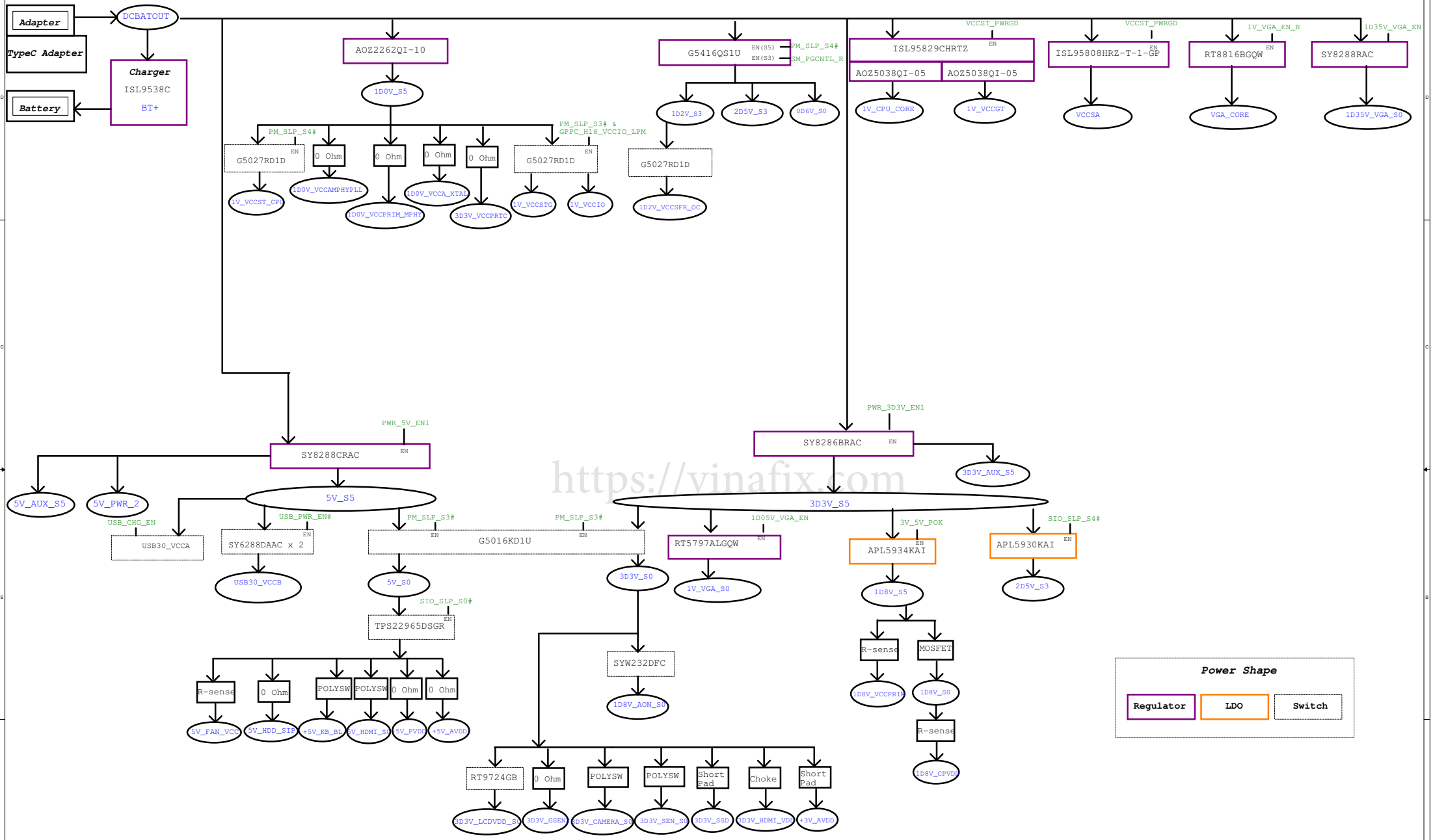
Power Sequence
Mockingbird CRB



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Title: Power Block Diagram

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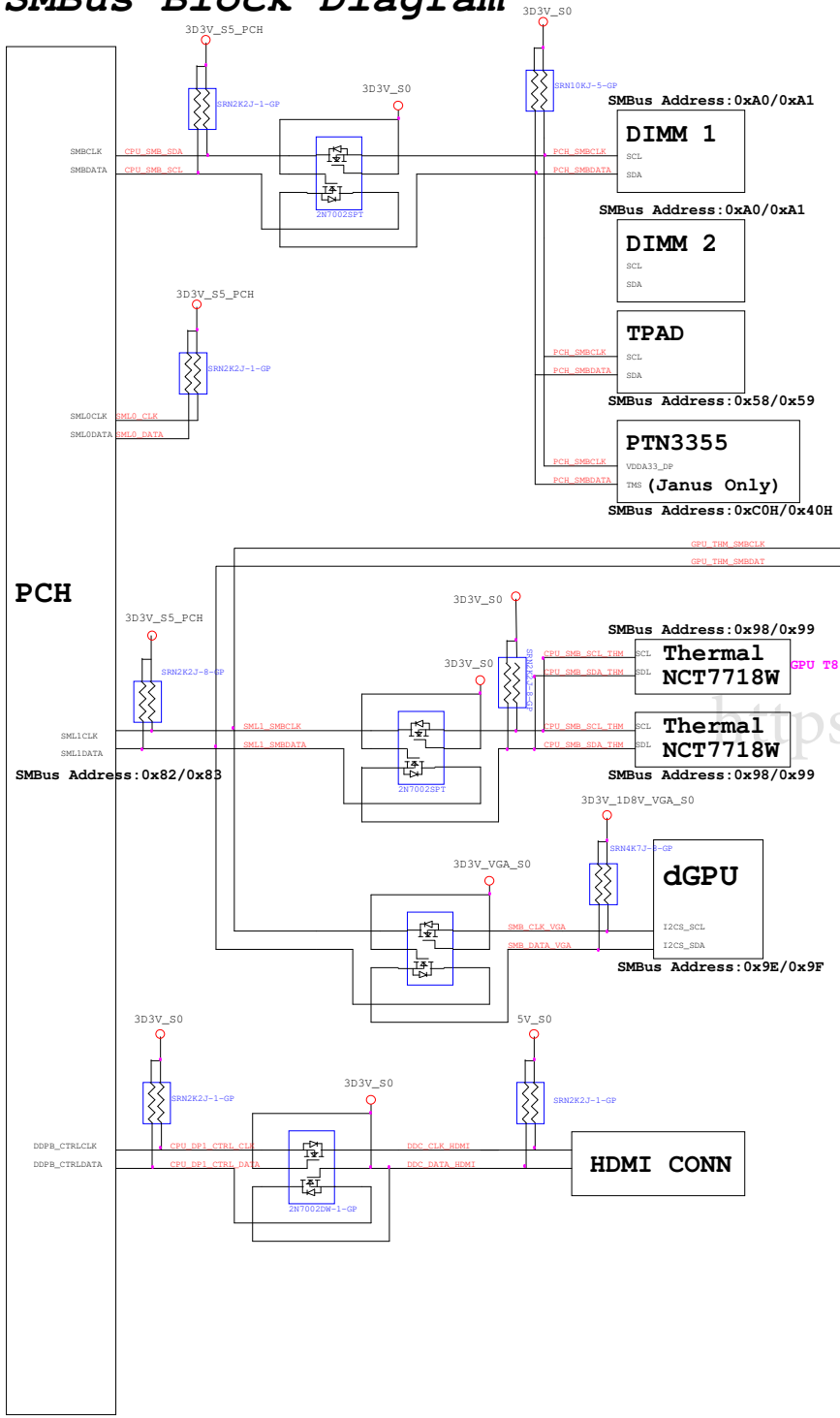
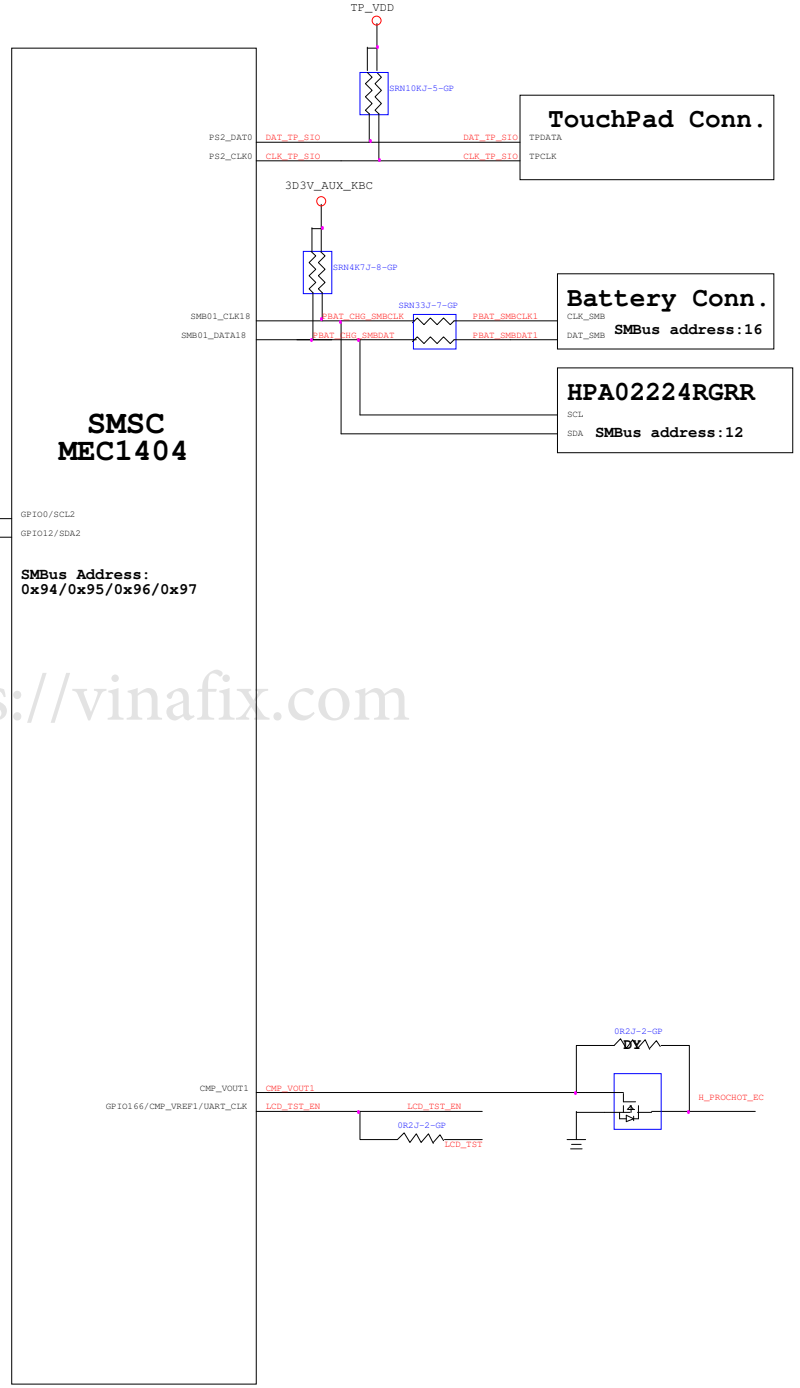
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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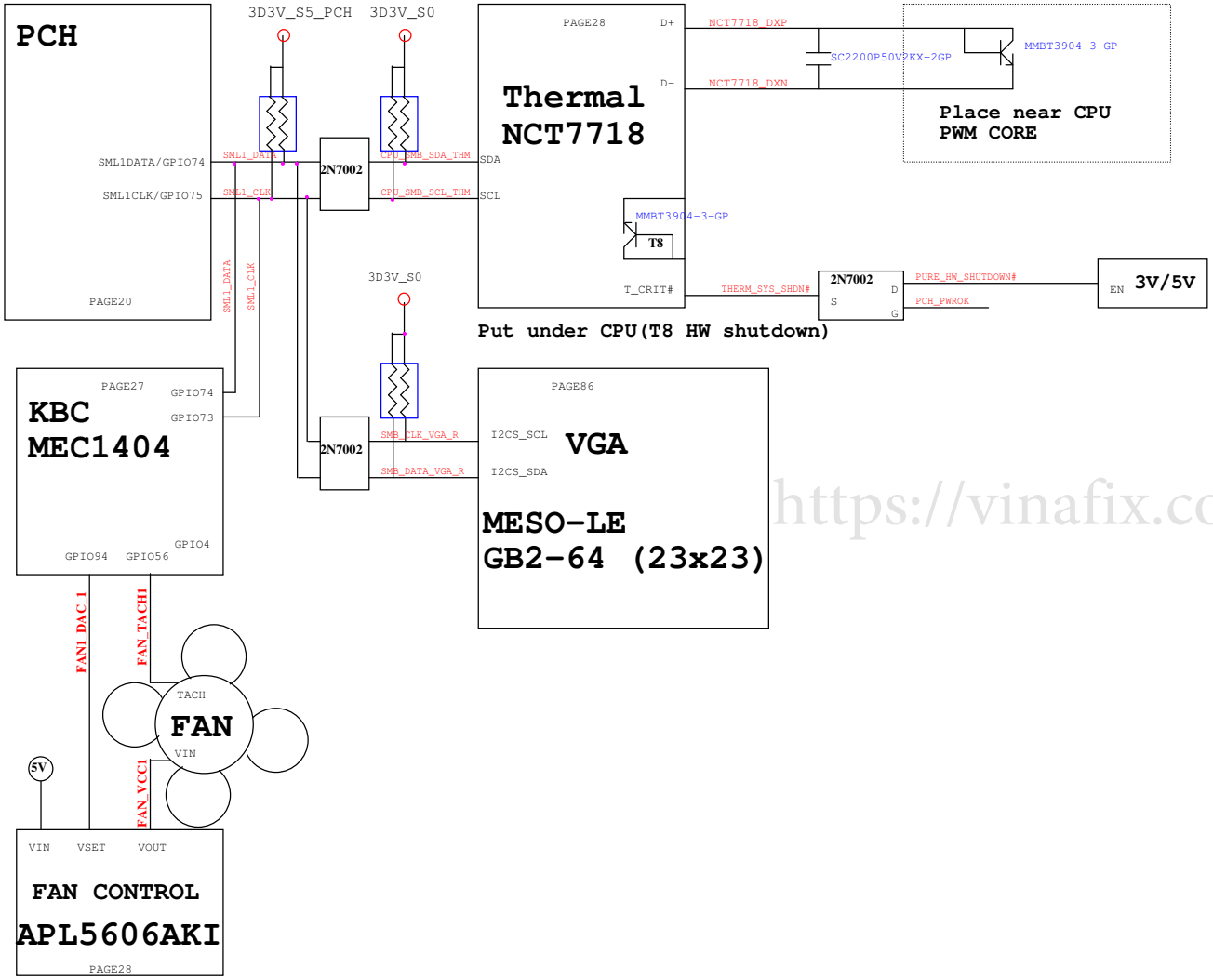
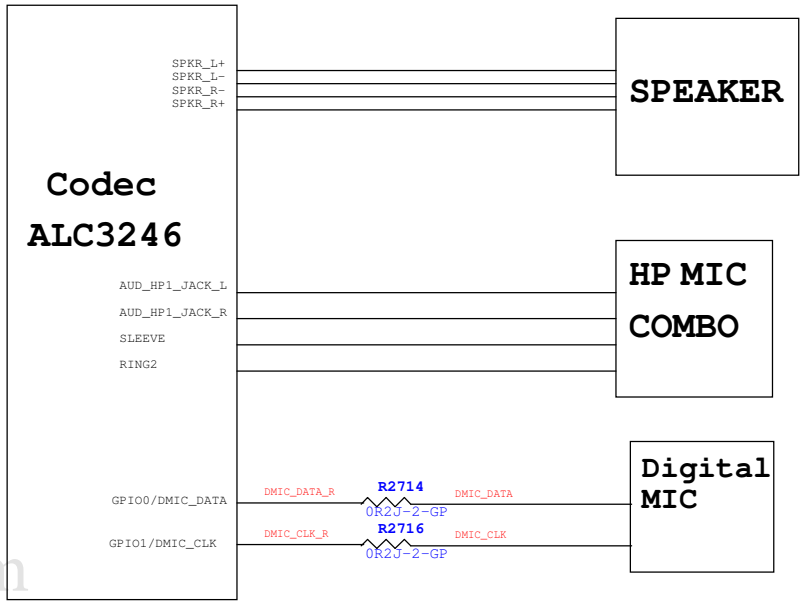
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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